

NASA-DoD Lead-Free Electronics Project
Plan
November 17, 2008

TABLE OF CONTENTS

1.0	BACKGROUND	6
2.0	GOALS.....	6
2.1	KEY QUESTION BEING ADDRESSED	6
3.0	STAKEHOLDERS	6
4.0	PROJECT MANAGEMENT.....	6
5.0	PROJECT ACTIVITIES	7
6.0	MATERIALS	8
6.1	SOLDER ALLOYS	8
6.1.1	SAC305 - Sn3.0Ag0.5Cu.....	8
6.1.2	SN100C – Sn0.7Cu0.05Ni($\leq 0.01\text{Ge}$)	8
6.2	FLUX	9
6.3	BOARD FINISH.....	10
6.4	COMPONENTS	10
7.0	COMPONENT CHARACTERIZATION.....	11
8.0	TEST VEHICLE ASSEMBLIES	11
8.1	BREAK-OFF COUPONS.....	11
8.1.1	Break-Off Coupon Breakdown.....	11
8.1.2	Break-Off Coupon Processing	14
8.1.3	Break-Off Coupon Pieces	14
8.2	TEST VEHICLE BREAK OUT	15
8.3	LEAD-FREE REWORK (BATCH A)	16
8.3.1	Bare Boards.....	16
8.3.2	Assembly Details.....	19
8.4	SNPb REWORK (BATCH B).....	21
8.4.1	Bare Boards.....	21
8.4.2	Assembly Details.....	24
8.5	SNPb MANUFACTURED (BATCH C)	27
8.5.1	Bare Boards.....	27
8.5.2	Assembly Details.....	29
8.6	SNPb MANUFACTURED (BATCH D).....	32
8.6.1	Bare Boards.....	32
8.6.2	Assembly Details.....	34
8.7	LEAD-FREE MANUFACTURED (BATCH E).....	37
8.7.1	Bare Boards.....	37
8.7.2	Assembly Details.....	39
8.8	LEAD-FREE MANUFACTURED (BATCH F).....	42
8.8.1	Bare Boards.....	42
8.8.2	Assembly Details.....	46
8.9	LEAD-FREE MANUFACTURED (BATCH G)	49
8.9.1	Bare Boards.....	49
8.9.2	Assembly Details.....	51
8.10	LEAD-FREE MANUFACTURED (BATCH H)	54
8.10.1	Bare Boards.....	54
8.10.2	Assembly Details.....	56
8.11	LEAD-FREE MANUFACTURED (BATCH I).....	58

8.11.1	<i>Bare Boards</i>	58
8.11.2	<i>Assembly Details</i>	61
9.0	AREA ARRAY X-RAY ANALYSIS	63
10.0	MANUFACTURED TEST VEHICLE CHARACTERIZATION	63
11.0	REWORK PROTOCOL	64
11.1	COMPONENT PREPARATION.....	70
11.1.1	<i>Moisture bake out per J-STD-033, table 4-1</i>	70
11.2	REWORK PROCEDURE PER IPC-7711.....	70
11.2.1	<i>Moisture bake out</i>	70
11.2.2	<i>Cleaning</i>	70
11.2.3	<i>Removal and Replacement</i>	70
12.0	THERMAL AGING, 100°C FOR 24 HOURS	74
13.0	REWORK TEST VEHICLE CHARACTERIZATION	74
14.0	TESTING ACTIVITIES	74
14.1	VIBRATION.....	75
14.2	THERMAL CYCLING.....	75
14.3	MECHANICAL SHOCK.....	75
14.4	COMBINED ENVIRONMENTS TEST.....	75
14.5	DROP TESTING.....	76
14.6	INTERCONNECT STRESS TEST (IST).....	76
14.7	COPPER DISSOLUTION.....	76
15.0	FAILURE ANALYSIS	77
15.1	PROCEDURE.....	77
15.1.1	<i>Sample Identification</i>	77
15.1.2	<i>Sample Size</i>	78
15.1.3	<i>FA/DPA Component Preparation</i>	81
15.1.4	<i>Analysis</i>	81
16.0	REFERENCES	83

List of Tables

Table 1 Project Activities.....	7
Table 2 Solder Alloy and Processes.....	8
Table 3 Solder Alloys and Associated Flux.....	9
Table 4 Components Table	10
Table 5 Test Vehicle Batch Key	15
Table 6 Test Vehicle Tracker– Lead-Free Rework Test Vehicles (Batch A).....	16
Table 7 Component Finish Matrix – Lead-Free Rework Test Vehicles (Batch A)**	17
Table 8 Test Vehicle Tracker - SnPb Rework Test Vehicles (Batch B).....	21
Table 9 Component Finish Matrix – SnPb Rework Test Vehicles (Batch B)**	22
Table 10 Test Vehicle Tracker – SnPb Manufactured Test Vehicles (Batch C)	27
Table 11 Component Finish Matrix – SnPb Manufactured Test Vehicles (Batch C)	28
Table 12 Test Vehicle Tracker – SnPb Manufactured Test Vehicles (Batch D)	32
Table 13 Component Finish Matrix – SnPb Manufactured Test Vehicles (Batch D)	32
Table 14 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles (Batch E)	37
Table 15 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch E).....	37
Table 16 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles (Batch F)	43
Table 17 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch F)	44
Table 18 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles (Batch G).....	49
Table 19 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch G)	49
Table 20 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles (Batch H).....	54
Table 21 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch H)	54
Table 22 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles (Batch I)	58
Table 23 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch I).....	58
Table 24 Manufactured Test Vehicles for Characterization	63
Table 25 Rework Test Vehicles for BAE Systems.....	64
Table 26 Rework Test Vehicles for Lockheed Martin.....	65
Table 27 Rework Test Vehicles for Rockwell Collins	65
Table 28 Component Finish Matrix – Lead-Free Rework (Batch A).....	66
Table 29 Component Finish Matrix – SnPb Rework (Batch B)	67
Table 30 Rework Test Vehicles for Characterization.....	74
Table 31 Example Failure Analysis Tracking Table (Batch C).....	79
Table 32 Example Failure Analysis Tracking Table (Batch B).....	80

List of Figures

Figure 1 Test Vehicle with Break-Off Coupon Attached	12
Figure 2 Test Vehicle with Break-Off Coupon Removed	13
Figure 3 Break-Off Coupon Pieces.....	14
Figure 4 Example Reflow Oven Profile - Lead-Free (SAC305)	19
Figure 5 Example Wave Solder Profile - Lead-Free (SN100C)	20
Figure 6 Example Reflow Oven Profile – Lead-Free (SAC305), being used for SnPb Rework Assemblies	25
Figure 7 Example Wave Solder Profile – Lead-Free (SN100C), being used for SnPb Rework Assemblies	26
Figure 8 Example Reflow Oven Profile (SnPb)	30
Figure 9 Example Wave Solder Profile (SnPb)	31
Figure 10 Example Reflow Oven Profile (SnPb)	35
Figure 11 Example Wave Solder Profile (SnPb)	36
Figure 12 Example Reflow Oven Profile - Lead-Free (SAC305)	40
Figure 13 Example Wave Solder Profile - Lead-Free (SN100C)	41
Figure 14 Example Reflow Oven Profile - Lead-Free (SAC305)	47
Figure 15 Example Wave Solder Profile - Lead-Free (SN100C)	48
Figure 16 Example Reflow Oven Profile - Lead-Free (SN100C)	52
Figure 17 Example Wave Solder Profile - Lead-Free (SN100C)	53
Figure 18 Example Reflow Oven Profile - Lead-Free (SN100C)	56
Figure 19 Example Wave Solder Profile - Lead-Free (SN100C)	57
Figure 20 Example Reflow Oven Profile - Lead-Free (SN100C)	61
Figure 21 Example Wave Solder Profile - Lead-Free (SN100C)	62
Figure 22 Rework Order = Batch A.....	68
Figure 23 - Rework Order = Batch B	69
Figure 24 Thermal Couple Map, Bottom Side of the Test Vehicle**	71
Figure 25 Example SnPb Rework Profile for area array components, removal and replacement	72
Figure 26 Example Lead-Free Rework Profile for area array components, removal and replacement	73
Figure 27 Failure Analysis Procedure.....	82

List of Appendices

Appendix A - TSOP components without dummy die	84
Appendix B - Example Component Characteristic Worksheet	86
Appendix C - Test Vehicle Drawings	87
Appendix D - NAVSEA Crane Assembly and Rework Effort.....	89
Appendix E - Mechanical Shock Procedure Change.....	91
Appendix F- Area Array X-Ray Analysis Parameters.....	98

1.0 [Background](#)

The Joint Council on Aging Aircraft and Joint Group on Pollution Prevention Lead-Free Solder Project (JCAA/JGPP LFS) began in 2001. The goal of the project was to study the effects of environmental testing on the relative reliability of lead-free and tin-lead (SnPb) solder joints and provide baseline data from the evaluation of lead-free solders and termination finishes. The testing conducted for that project generated critical reliability data for aerospace and defense applications as documented in the Joint Test Report (JTR). A copy of the JTR can be found on the NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center [website](#).

The NASA-DoD Lead-Free Electronics Project testing will build on the results from the JCAA/JGPP LFS Project focusing on the rework (Rwk.) of SnPb and lead-free solder alloys and will include the mixing of SnPb and lead-free solder alloys. The majority of testing being conducted for this effort will mirror the testing completed for JCAA/JGPP LFS Project. Some changes were made in order to optimize the usefulness of the data. The Joint Test Protocol for the NASA-DoD Lead-Free Electronics Project can be found on the NASA TEERM [website](#).

2.0 [Goals](#)

- Generate reliability data for circuit cards manufactured and reworked with SnPb and lead-free solders and subjected to rigorous environmental exposure conditions.
- Provide baseline data for aerospace and defense (high-reliability) applications.

2.1 **Key Question Being Addressed**

To what extent do rework procedures, including SnPb and lead-free mixed solder joints, affect solder joint reliability of high-performance electronics using SnPb as a baseline?

3.0 [Stakeholders](#)

The following is a list of participating stakeholders:

- | | | |
|----------------|--------------------|------------------------------|
| • NASA | • Rockwell Collins | • Celestica |
| • DMEA | • Boeing | • Texas Instruments |
| • NAVSEA-Crane | • BAE Systems | • Honeywell |
| • Air Force | • Lockheed Martin | • Scorpio Solutions |
| • Raytheon | • Harris | • Nihon Superior |
| • ITB, Inc. | • COM DEV | • PWB Interconnect Solutions |

4.0 [Project Management](#)

The project is being managed by Kurt Kessel from the NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center.

5.0 [Project Activities](#)

Table 1 Project Activities

Project Activity	Responsible Party
Procurement	
Procurement of components and boards, includes tinning of component leads	NAVSEA Crane Lockheed Martin
Component Characterization	
Component Characterization	Rockwell Collins COM DEV Boeing
Assembly	
Surface Mount Assembly and SnPb wave soldering	BAE Systems
Lead-free wave soldering	Scorpio Solutions
Assembly Characterization	
1 test vehicle from each of the 4 test vehicle types assembled	Rockwell Collins
Assembly Inspection	
In-line x-ray evaluation of test vehicle assemblies	Lockheed Martin
Rework	
Extra, Characterization, Vibration and Combined Environments Test Vehicles	BAE Systems
Thermal Cycle, -55 to +125°C and -20 to +80°C Test Vehicles	Lockheed Martin
Mechanical Shock and Drop Testing Test Vehicles	Rockwell Collins
Rework Characterization	
1 component from each of the 4 component types (BGA, CSP, PDIP, TSOP) being reworked from each of the 3 types of rework boards (SnPb, SnPb-ENIG, LF).	Rockwell Collins
Thermal Aging	
All test vehicles to be aged, 100°C for 24 hours	BAE Systems
Testing	
Thermal Cycling -55 to +125°C	Rockwell Collins
Thermal Cycling -20 to +80°C	Boeing
Vibration	Boeing
Combined Environments	Raytheon
Drop Testing	Celestica
Mechanical Shock	Boeing / Nihon Superior
Interconnect Stress Testing (IST)	PWB Interconnect Solutions
Failure Analysis	
Micro-section analysis	Celestica
Micro-section analysis	COM DEV
Micro-section analysis	Harris
Micro-section analysis	Lockheed Martin
Micro-section analysis – Thermal Cycle -55 to +125°C	Rockwell Collins
Micro-section analysis	NASA-MSFC

6.0 [Materials](#)

6.1 Solder Alloys

The lead-free solder alloys selected for this project are:

- SAC305 – Sn3.0Ag0.5Cu – reflow soldering
 - Tin (Sn); Silver (Ag); Copper (Cu)
- SN100C - Sn-0.7Cu-0.05Ni + Ge - reflow and wave soldering
 - Tin (Sn); Copper (Cu); Nickel (Ni); Germanium (Ge)

Selection criteria of prime importance included commercial availability, industry trends, and past reliability testing performance.

Table 2 Solder Alloy and Processes

Solder Alloy	Solder Process		
	Reflow	Wave	Manual
SAC305	X	N/A	X
SN100C	X	X	X
SnPb baseline	X	X	X

N/A = Due to limitations on board numbers and components, these solder alloys were not used during the noted assembly processes

6.1.1 SAC305 - Sn3.0Ag0.5Cu

SnAgCu solder alloys are believed to be the leading choice of the commercial electronics industry for lead-free solder. The Sn3.0Ag0.5Cu is recommended by industry and research consortia as a prime candidate for replacing SnPb solder. Sn3.0Ag0.5Cu is commercially available and currently used in electronic applications. It has been determined that alloys with compositions within the range of Sn3.0-4.0Ag0.5-1.0Cu all have a liquidus temperature around 217°C and have similar microstructures and mechanical properties.

This alloy was chosen for reflow soldering because this particular solder alloy has shown the most promise as a primary replacement for tin-lead solder. The team decided that they wanted to select at least one “general purpose” alloy to be evaluated and it was determined that the SnAgCu solder alloy would best serve this purpose. Conclusions drawn from literature suggest that this alloy has good mechanical properties and may be as reliable as SnPb in some applications.

BAE Systems reviewed several SAC305 solder alloys for printing, reflow, and cleaning characteristics before choosing EnviroMark™ 907 from Kester.

6.1.2 SN100C – Sn0.7Cu0.05Ni(≤0.01Ge)

This alloy is commercially available and the general trend in industry has been to switch to the nickel stabilized tin-copper alloy over standard tin-copper due to its superior performance. In addition, this nickel-stabilized alloy does not require special solder pots and has shown no joint failures in specimens with over four (4) years of service. The cost

of this alloy in the form of bar solder is relatively low when compared to other lead-free solder alloys in bar form.

The superior performance of the tin-copper-nickel alloy has been confirmed by university research which has found that the nickel addition works by facilitating solidification of the alloy as a fine uniform eutectic structure and suppressing the growth of primary tin dendrites that are the cause of shrinkage defects in the unmodified alloy. This mode of solidification enhances the fluidity of the alloy close to the melting point, a property that is important in a solder so that it is comparable with that of tin-lead solder at the same superheat. The tin-copper-nickel alloy is representative of a new class of modified tin-copper solders that are increasing in popularity as the limitations of the tin-silver-copper alloys in some applications become apparent.

Nihon Superior SN100C will be used for this project.

6.2 Flux

The flux systems used during soldering were "low residue" or no-clean fluxes and the group chose to clean the test vehicles after processing even though no-clean fluxes were used with some solders. Additionally, reflow was accomplished without nitrogen inerting, which might have created a smaller soldering process window (a credit to the BAE Systems crew for creating a quality test vehicle under such tough process conditions).

Table 3 Solder Alloys and Associated Flux

Solder Alloy	Flux		
	Reflow Soldering	Wave Soldering	Manual Soldering
SAC305	ROL1	N/A	R Heat Stabilized Resin ROL0 Tacky Flux
SN100C	ROL0	ORL0	R Heat Stabilized Resin ROL0 Tacky Flux
SnPb baseline	ROL0	Type ORM0	ORL0 ROL0 Tacky Flux

Table provided by BAE Systems Irving, Texas

N/A = Due to limitations on board numbers and components, these solder alloys were not used during the noted assembly processes

R = Rosin Base

ROL0 = Rosin, Low or no flux/flux residue activity, no halide present

ROL1 = Rosin, Low or no flux/flux residue activity, halide present

ORM0 = Organic, Moderate flux/flux residue activity, no halide present

6.3 Board Finish

Project stakeholders and participants selected immersion silver (Enthone Alphastar Ag) as the surface finish for the majority of the test vehicles. The consensus of the project team was that immersion silver has the best balance of desirable properties: good wetting by solders, good solder joint reliability, good long-term solderability upon storage, and retention of solderability after multiple reflow cycles. In addition, several major electronic manufacturing companies are currently using immersion silver in production.

A limited number of test vehicles were assembled using an Electroless Nickel Immersion Gold (ENIG) surface finish (Uyemura Kat 450 ENIG). The project stakeholders felt that ENIG would be a good secondary surface finish since it provides good planarity and solderability which can withstand multiple reflows. ENIG has also been shown to perform well with regards to; substrate shelf-life, corrosion resistance, assembly process window, thermal resistance over several temperature excursions, and good reworkability.

6.4 Components

The project stakeholder's agreed to populate the test vehicles with the following components:

Table 4 Components Table

20LCC-1.27mm-8.90mm-DC-L-Au = Tinning-SAC305
20LCC-1.27mm-8.90mm-DC-L-Au = Tinning-SnPb
A-MLF20-5mm-.65mm-DC(30467)
A-MLF20-5mm-.65mm-DC-Sn(30801)
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643)
A-TQFP144-20mm-.5mm-2.0-DC-NiPdAu
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = Tinning-SAC305
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = Tinning-SnPb
PBGA225-1.5mm-27mm-DC(10565)
PBGA225-1.5mm-27mm-DC-LF(16074)
A-PDIP20T-7.6mm-DC-Sn (30737)
PDIP20T-DC (12006)
PDIP-20 - NiPdAu
A-CABGA100-.8mm-10mm-DC(30102)
A-CABGA100-.8mm-10mm-DC-LF(30695)
A-CABGA100-.8mm-10mm-DC-105
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-SnBi-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-Sn-TR

Note – The TSOP-50 components do not have a dummy die. For more information on the decision not to include dummy die, please see Appendix A

7.0 Component Characterization

Destructive Physical Analysis (DPA) will be performed on samples from each of the component types being placed onto the test vehicles. The DPA process is being used to ensure that the components being used for testing meet the consortia required standards and to evaluate the quality of construction. A worksheet (Appendix B) has been developed to ensure that all locations performing DPA collect the same information.

8.0 Test Vehicle Assemblies

The following section has been organized by how BAE Systems will process the test vehicles.

8.1 Break-Off Coupons

Break-off coupons will be divided into two groups, those that will be processed through reflow and wave solder processing and those that will be removed prior to reflow and wave solder processing. The break-off coupons will be divided by [Batch](#).

8.1.1 Break-Off Coupon Breakdown

8.1.1.1 Break-off coupons that will remain during soldering

Break-off coupons will remain on the following test vehicles through reflow and wave solder processing:

- Lead-Free Rework (Batch A)
- SnPb Manufactured (Batch C)
- Lead-Free Manufactured (Batch E)
- Lead-Free Manufactured (Batch G)
- Lead-Free Manufactured (Batch H)
- Lead-Free Manufactured (Batch I)

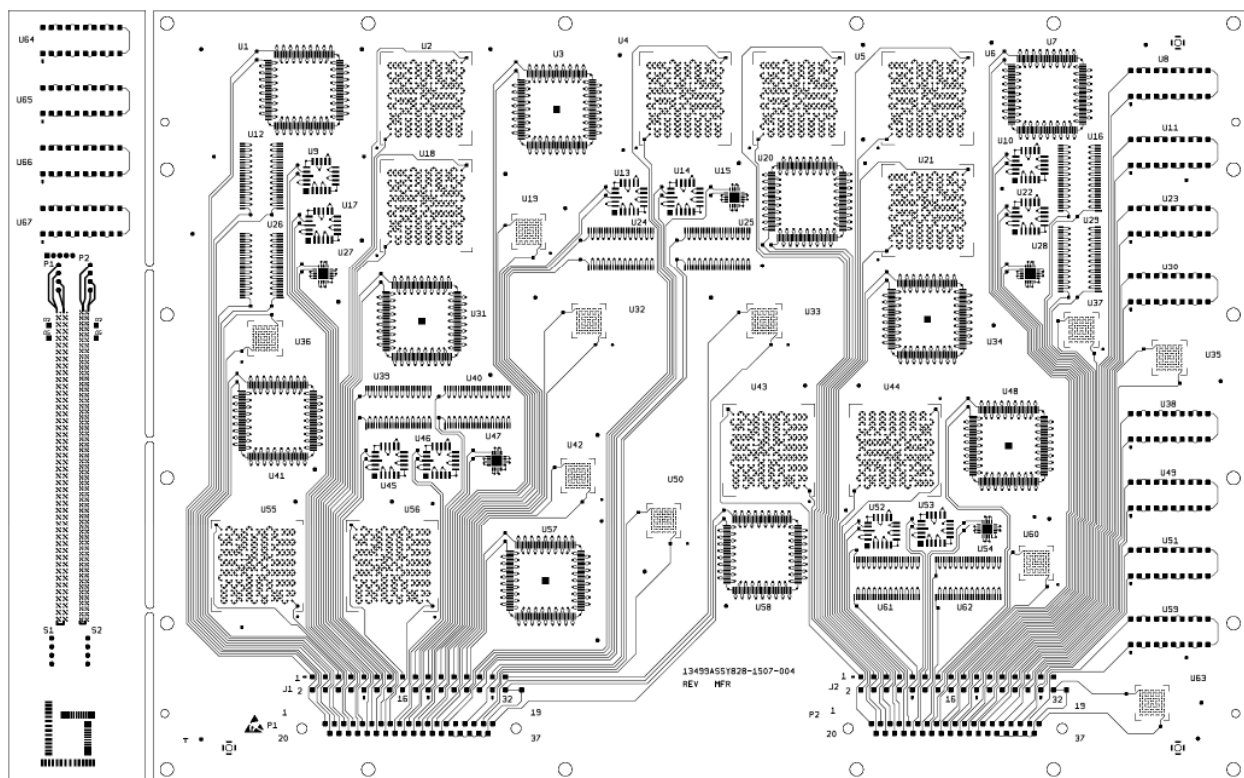


Figure 1 Test Vehicle with Break-Off Coupon Attached

8.1.1.2 Break-off coupons that will be removed before soldering

Break-off coupons will be removed from the following test vehicles prior to reflow and wave solder processing:

- SnPb Rework (Batch B)
- SnPb Manufactured (Batch D)
- Lead-Free Manufactured (Batch F)

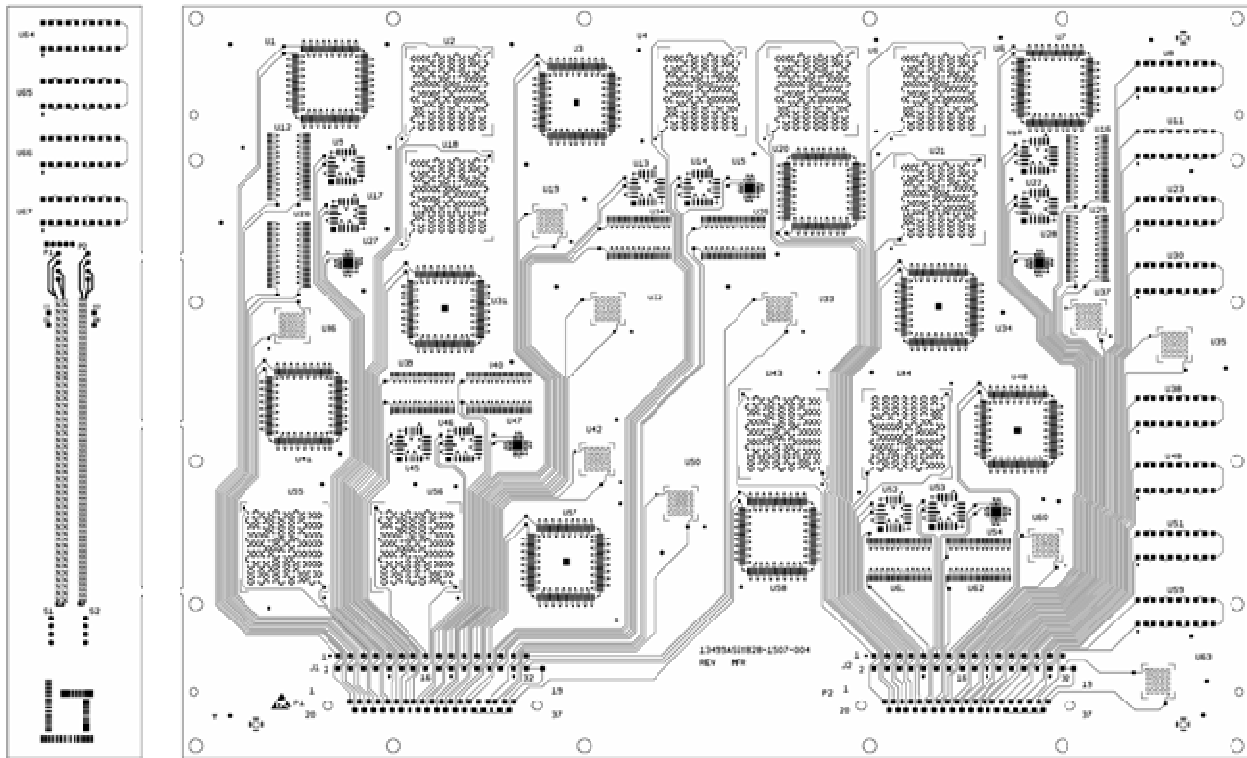


Figure 2 Test Vehicle with Break-Off Coupon Removed

8.1.2 Break-Off Coupon Processing

- Break-off coupons that go through lead-free reflow and wave soldering will be removed by Scorpio Solutions and shipped to BAE Systems for capacitance measurements. BAE Systems will then ship the break-off coupons to Rockwell Collins to be divided into three separate pieces, two copper dissolution coupons and one IST coupon.
- Break-off coupons that go through SnPb reflow and wave soldering will be removed by BAE Systems and shipped to Rockwell Collins to be divided into the three separate pieces.
- Break-off coupons that will not be processed through reflow solder processing will be removed by BAE Systems and shipped to PWB Interconnect Solutions for IST testing.

8.1.3 Break-Off Coupon Pieces

- a. Copper dissolution coupon (plated through hole). The plated through hole pattern has serial reduction in hole size to simulate the various aspect ratios possible in through-hole soldering and the effects of the barrel (plated copper) when exposed to rework conditions. Additional details are contained in the in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.
- b. IST coupon. Coupons are designed to determine if thermal processing degrades via reliability and promotes board delamination. Additional details are contained in the in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.
- c. Copper dissolution coupon (surface trace). The surface trace feature (Foil copper) of the coupon has been included to evaluate the effect on surface features exposed to rework. Additional details are contained in the in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

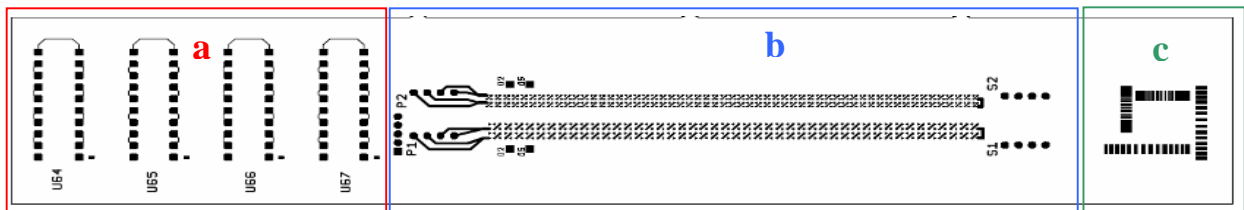


Figure 3 Break-Off Coupon Pieces

8.2 Test Vehicle Break Out

Due to the various types of test vehicles being assembled, BAE Systems will assemble the test vehicles in multiple batches.

Table 5 Test Vehicle Batch Key

Test Vehicle Type	Reflow Solder	Wave Solder	Batch (Section Number)	Serial Numbers	Number of Boards
Lead-Free Rework All Test Vehicles	SAC305	SN100C	A (8.3)	161-193	33
SnPb Rework* All Test Vehicles	SnPb*	SnPb*	B (8.4)	121-160	40
SnPb Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SnPb	SnPb	C (8.5)	1, 3, 5-14, 20 - 24	17
SnPb Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SnPb	SnPb	D (8.6)	2, 4, 15-19, 25-34	17
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SAC305	SN100C	E (8.7)	35, 39, 41-45, 50-54, 69-73, 93, 95, 97	20
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SAC305	SN100C	F (8.8)	36-38, 40, 46-49, 55-68, 74-92, 94, 96	43
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SN100C	SN100C	G (8.9)	100, 102-106, 116-120	11
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SN100C	SN100C	H (8.10)	101, 111-115	6
Lead-Free Manufactured Test Vehicles Crane Rework Effort	SN100C	SN100C	I (8.11)	98-99, 107-110	6

* NOTE: Lead-Free profiles will be used for reflow and wave soldering

8.3 Lead-Free Rework ([Batch A](#))

8.3.1 Bare Boards

- 33 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 6 Test Vehicle Tracker– Lead-Free Rework Test Vehicles ([Batch A](#))

Project Activity	Board Number	Board Finish
Extra Boards	SN161	Immersion Ag
	SN162	
Test Vehicle Characterization	SN163	
Thermal Cycling: -55C to +125C	SN164	
	SN165	
	SN166	
	SN167	
	SN168	
Thermal Cycling: -20C to +80C	SN169	
	SN170	
	SN171	
	SN172	
	SN173	
Vibration	SN174	
	SN175	
	SN176	
	SN177	
	SN178	
Combined Environments Testing	SN179	
	SN180	
	SN181	
	SN182	
	SN183	
Drop Testing	SN184	
	SN185	
	SN186	
	SN187	
	SN188	
Mechanical Shock	SN189	
	SN190	
	SN191	
	SN192	
	SN193	

Table 7 Component Finish Matrix – Lead-Free Rework Test Vehicles ([Batch A](#))**

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U18	BGA-225	SAC405	SAC305	
U43	BGA-225	SAC405	SAC305	
U06	BGA-225	SAC405	SAC305	
U02	BGA-225	SAC405	SAC305	
U21	BGA-225	SAC405	SAC305	
U56	BGA-225	SAC405	SAC305	
U04	BGA-225	SnPb	SAC305	
U55	BGA-225	SnPb	SAC305	
U05	BGA-225	SnPb	SAC305	
U44	BGA-225	SnPb	SAC305	
U09	CLCC-20	SnPb	SAC305	
U13	CLCC-20	SnPb	SAC305	
U22	CLCC-20	SnPb	SAC305	
U46	CLCC-20	SnPb	SAC305	
U53	CLCC-20	SnPb	SAC305	
U10	CLCC-20	SnPb	SAC305	
U14	CLCC-20	SnPb	SAC305	
U17	CLCC-20	SnPb	SAC305	
U45	CLCC-20	SnPb	SAC305	
U52	CLCC-20	SnPb	SAC305	
U33	CSP-100	SAC105	SAC305	
U50	CSP-100	SAC105	SAC305	
U19	CSP-100	SAC105	SAC305	
U37	CSP-100	SAC105	SAC305	
U42	CSP-100	SAC105	SAC305	
U60	CSP-100	SAC105	SAC305	
U36	CSP-100	SAC105	SAC305	
U32	CSP-100	SnPb	SAC305	
U35	CSP-100	SnPb	SAC305	
U63	CSP-100	SnPb	SAC305	
U08	PDIP-20	Sn		SN100C
U23	PDIP-20	Sn		SN100C
U49	PDIP-20	Sn		SN100C
U59	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U11	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	SnPb	SAC305	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U27	QFN	SnPb	SAC305	
U28	QFN	SnPb	SAC305	
U47	QFN	SnPb	SAC305	
U54	QFN	SnPb	SAC305	
U03	TQFP-144	NiPdAu	SAC305	
U31	TQFP-144	NiPdAu	SAC305	
U34	TQFP-144	NiPdAu	SAC305	
U48	TQFP-144	NiPdAu	SAC305	
U57	TQFP-144	NiPdAu	SAC305	
U01	TQFP-144	SAC 305 Dip	SAC305	
U07	TQFP-144	SAC 305 Dip	SAC305	
U20	TQFP-144	SAC 305 Dip	SAC305	
U41	TQFP-144	SAC 305 Dip	SAC305	
U58	TQFP-144	SAC 305 Dip	SAC305	
U12	TSOP-50	Sn	SAC305	
U25	TSOP-50	Sn	SAC305	
U29	TSOP-50	SnBi	SAC305	
U39	TSOP-50	SnBi	SAC305	
U61	TSOP-50	SnBi	SAC305	
U24	TSOP-50	SnBi	SAC305	
U26	TSOP-50	SnBi	SAC305	
U16	TSOP-50	SnPb	SAC305	
U40	TSOP-50	SnPb	SAC305	
U62	TSOP-50	SnPb	SAC305	

** This table shows the termination finishes and solder alloys being used for initial manufacturing only. See Table 28 for the termination finishes and solder alloys being used for rework.

8.3.2 Assembly Details

- Reflow Soldering
- Location – BAE Systems Irving, Texas
- Reflow Profile = SAC305
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Soldering
- Location – Scorpio Solutions
- Wave Profile = SN100C
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 155°C to 175°C
 - Speed: 90 cm/min

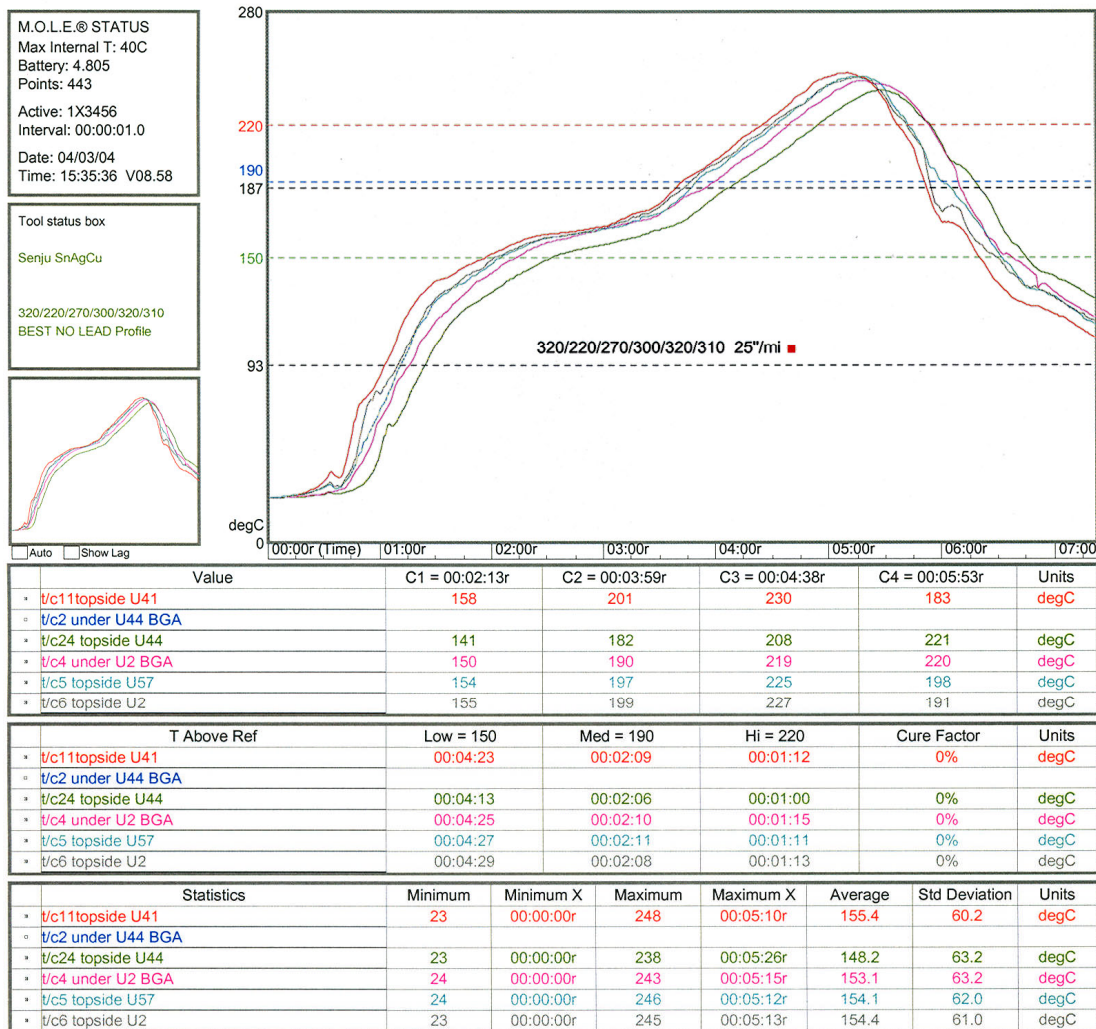
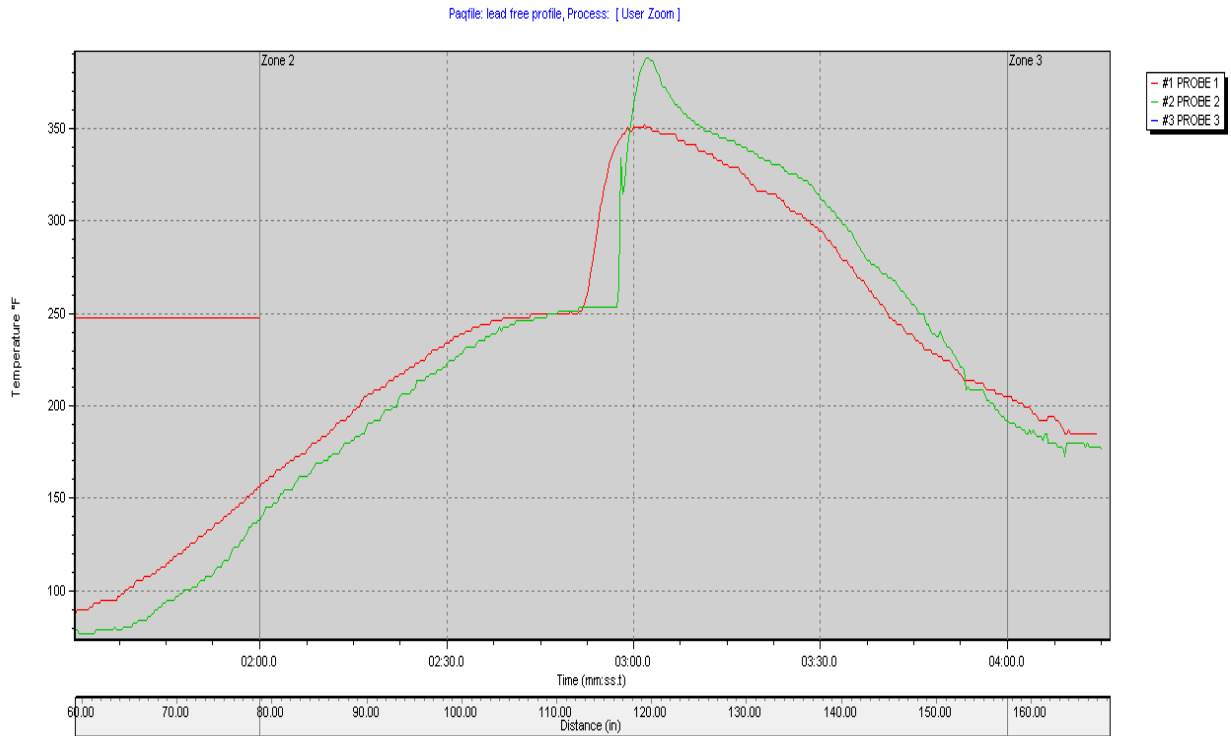


Figure 4 Example Reflow Oven Profile - Lead-Free (SAC305)



Reflow Results					
Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	***	***	00:00.0	***	

Figure 5 Example Wave Solder Profile - Lead-Free (SN100C)

8.4 SnPb Rework ([Batch B](#))

8.4.1 Bare Boards

- 40 boards
- 14.5"X 9"X 0.09"
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag and ENIG surface finishes

Table 8 Test Vehicle Tracker - SnPb Rework Test Vehicles ([Batch B](#))

Project Activity	Board Number	Board Finish	Board Number	Board Finish
Extra Boards	SN121	Immersion Ag	N/A	ENIG
	SN122			
Test Vehicle Characterization	SN123		SN154	
Thermal Cycling: -55C to +125C	SN124		SN155	
	SN125			
	SN126			
	SN127			
	SN128			
Thermal Cycling: -20C to +80C	SN129		SN156	
	SN130			
	SN131			
	SN132			
	SN133			
Vibration	SN134		SN157	
	SN135			
	SN136			
	SN137			
	SN138			
Combined Environments Testing	SN139		SN158	
	SN140			
	SN141			
	SN142			
	SN143			
Drop Testing	SN144		SN159	
	SN145			
	SN146			
	SN147			
	SN148			
Mechanical Shock	SN149		SN160	
	SN150			
	SN151			
	SN152			
	SN153			

Table 9 Component Finish Matrix – SnPb Rework Test Vehicles (Batch B)**

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U04	BGA-225	SAC405	SnPb	
U55	BGA-225	SAC405	SnPb	
U05	BGA-225	SAC405	SnPb	
U44	BGA-225	SAC405	SnPb	
U18	BGA-225	SnPb	SnPb	
U43	BGA-225	SnPb	SnPb	
U06	BGA-225	SnPb	SnPb	
U02	BGA-225	SnPb	SnPb	
U21	BGA-225	SnPb	SnPb	
U56	BGA-225	SnPb	SnPb	
U09	CLCC-20	SAC305	SnPb	
U13	CLCC-20	SAC305	SnPb	
U22	CLCC-20	SAC305	SnPb	
U46	CLCC-20	SAC305	SnPb	
U53	CLCC-20	SAC305	SnPb	
U10	CLCC-20	SAC305	SnPb	
U14	CLCC-20	SAC305	SnPb	
U17	CLCC-20	SAC305	SnPb	
U45	CLCC-20	SAC305	SnPb	
U52	CLCC-20	SAC305	SnPb	
U32	CSP-100	SAC105	SnPb	
U35	CSP-100	SAC105	SnPb	
U63	CSP-100	SAC105	SnPb	
U36	CSP-100	SAC105	SnPb	
U33	CSP-100	SnPb	SnPb	
U50	CSP-100	SnPb	SnPb	
U19	CSP-100	SnPb	SnPb	
U37	CSP-100	SnPb	SnPb	
U42	CSP-100	SnPb	SnPb	
U60	CSP-100	SnPb	SnPb	
U08	PDIP-20	NiPdAu		SnPb
U23	PDIP-20	NiPdAu		SnPb
U49	PDIP-20	NiPdAu		SnPb
U59	PDIP-20	Sn		SnPb
U30	PDIP-20	Sn		SnPb
U38	PDIP-20	Sn		SnPb
U11	PDIP-20	SnPb		SnPb
U51	PDIP-20	SnPb		SnPb
U15	QFN	Matte Sn	SnPb	
U27	QFN	Matte Sn	SnPb	
U28	QFN	Matte Sn	SnPb	
U47	QFN	Matte Sn	SnPb	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U54	QFN	Matte Sn	SnPb	
U03	TQFP-144	NiPdAu	SnPb	
U31	TQFP-144	NiPdAu	SnPb	
U34	TQFP-144	NiPdAu	SnPb	
U48	TQFP-144	NiPdAu	SnPb	
U57	TQFP-144	NiPdAu	SnPb	
U01	TQFP-144	SnPb Dip	SnPb	
U07	TQFP-144	SnPb Dip	SnPb	
U20	TQFP-144	SnPb Dip	SnPb	
U41	TQFP-144	SnPb Dip	SnPb	
U58	TQFP-144	SnPb Dip	SnPb	
U29	TSOP-50	Sn	SnPb	
U39	TSOP-50	Sn	SnPb	
U61	TSOP-50	Sn	SnPb	
U16	TSOP-50	SnBi	SnPb	
U40	TSOP-50	SnBi	SnPb	
U62	TSOP-50	SnBi	SnPb	
U12	TSOP-50	SnPb	SnPb	
U25	TSOP-50	SnPb	SnPb	
U24	TSOP-50	SnPb	SnPb	
U26	TSOP-50	SnPb	SnPb	

** This table shows the termination finishes and solder alloys being used for manufacturing only. See Table 29 for the termination finishes and solder alloys being used for rework.

8.4.2 Assembly Details

The NASA-DoD Lead-Free Electronics Project consortia members agreed to use higher temperature lead-free reflow and wave soldering profiles in conjunction with SnPb solder alloys for the SnPb Rework Test Vehicles only. The intent is to ensure complete mixing of the SnPb solder paste with the SAC BGA balls which should maximize reliability. Incomplete solder mixing within lead-free solder balls attached with SnPb solder using a SnPb reflow profile is known to give reduced reliability for area array components [1-2].

- Reflow Soldering
- Location - BAE Systems Irving, Texas
- Reflow Profile = SAC305
 - Preheat = 60-120 seconds @150-190°C
 - Peak temperature target = 243°C
 - Reflow:~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Soldering
- Location - BAE Systems Irving, Texas
- Wave Profile = SN100C
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

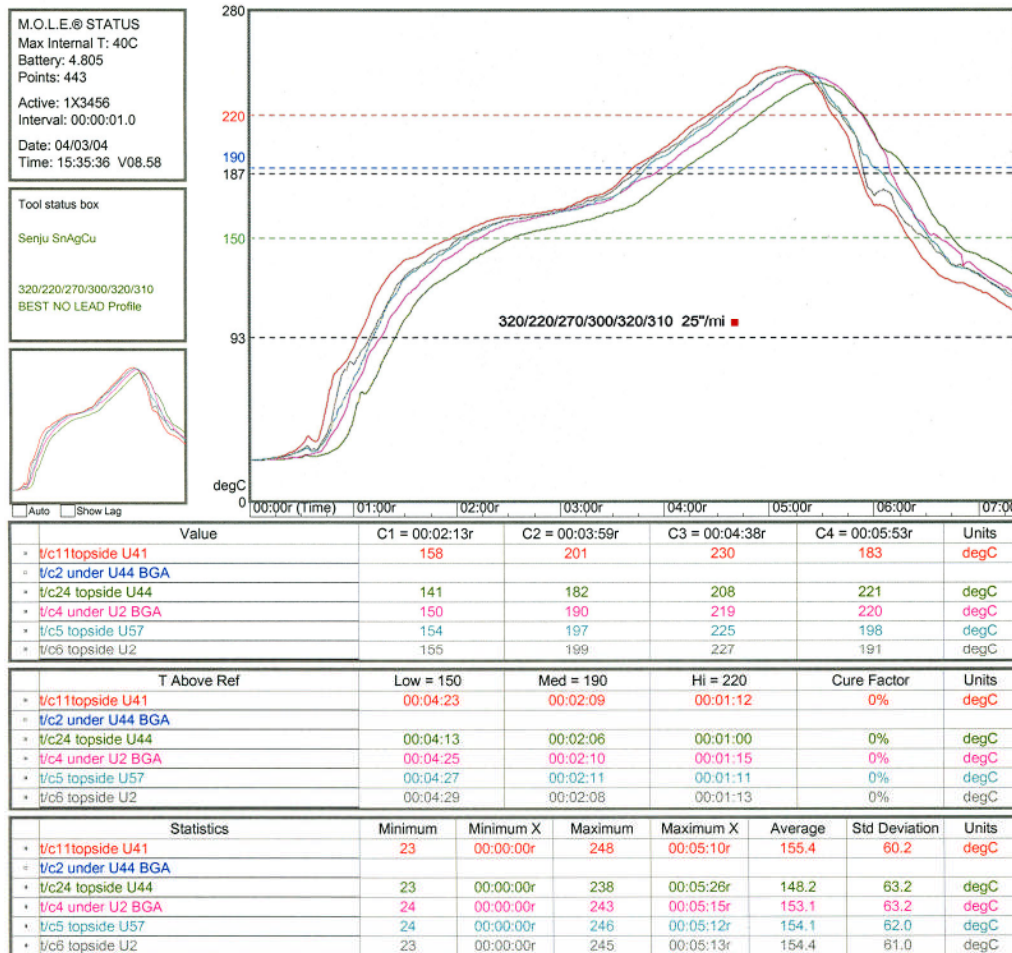
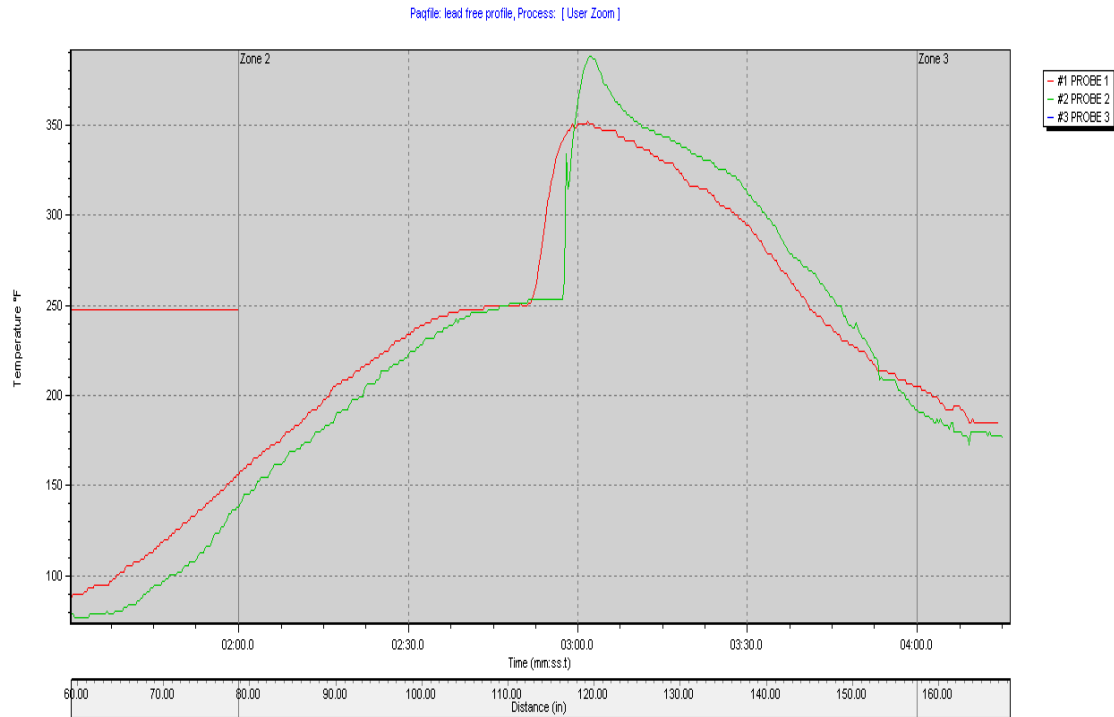


Figure 6 Example Reflow Oven Profile – Lead-Free (SAC305), being used for SnPb Rework Assemblies



Reflow Results					
Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	***	***	00:00.0	***	

Figure 7 Example Wave Solder Profile – Lead-Free (SN100C), being used for SnPb Rework Assemblies

8.5 SnPb Manufactured ([Batch C](#))

8.5.1 Bare Boards

- 17 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 10 Test Vehicle Tracker – SnPb Manufactured Test Vehicles ([Batch C](#))

Project Activity	Board Number	Board Finish
Extra Boards	SN1	Immersion Ag
Test Vehicle Characterization	SN3	
Thermal Cycling: -55C to +125C	SN5	
	SN6	
	SN7	
	SN8	
	SN9	
Thermal Cycling: -20C to +80C	SN10	
	SN11	
	SN12	
	SN13	
	SN14	
Combined Environments Testing	SN20	
	SN21	
	SN22	
	SN23	
	SN24	

Table 11 Component Finish Matrix – SnPb Manufactured Test Vehicles ([Batch C](#))

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U18	BGA-225	SAC405	SnPb	
U43	BGA-225	SAC405	SnPb	
U04	BGA-225	SAC405	SnPb	
U06	BGA-225	SAC405	SnPb	
U55	BGA-225	SAC405	SnPb	
U02	BGA-225	SnPb	SnPb	
U05	BGA-225	SnPb	SnPb	
U21	BGA-225	SnPb	SnPb	
U44	BGA-225	SnPb	SnPb	
U56	BGA-225	SnPb	SnPb	
U09	CLCC-20	SAC305	SnPb	
U13	CLCC-20	SAC305	SnPb	
U22	CLCC-20	SAC305	SnPb	
U46	CLCC-20	SAC305	SnPb	
U53	CLCC-20	SAC305	SnPb	
U10	CLCC-20	SnPb	SnPb	
U14	CLCC-20	SnPb	SnPb	
U17	CLCC-20	SnPb	SnPb	
U45	CLCC-20	SnPb	SnPb	
U52	CLCC-20	SnPb	SnPb	
U32	CSP-100	SAC105	SnPb	
U33	CSP-100	SAC105	SnPb	
U35	CSP-100	SAC105	SnPb	
U50	CSP-100	SAC105	SnPb	
U63	CSP-100	SAC105	SnPb	
U19	CSP-100	SnPb	SnPb	
U36	CSP-100	SnPb	SnPb	
U37	CSP-100	SnPb	SnPb	
U42	CSP-100	SnPb	SnPb	
U60	CSP-100	SnPb	SnPb	
U08	PDIP-20	NiPdAu		SnPb
U23	PDIP-20	NiPdAu		SnPb
U49	PDIP-20	NiPdAu		SnPb
U59	PDIP-20	NiPdAu		SnPb
U11	PDIP-20	Sn		SnPb
U30	PDIP-20	Sn		SnPb
U38	PDIP-20	Sn		SnPb
U51	PDIP-20	Sn		SnPb
U15	QFN	Matte Sn	SnPb	
U27	QFN	Matte Sn	SnPb	
U28	QFN	Matte Sn	SnPb	
U47	QFN	Matte Sn	SnPb	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U54	QFN	Matte Sn	SnPb	
U01	TQFP-144	Matte Sn	SnPb	
U07	TQFP-144	Matte Sn	SnPb	
U20	TQFP-144	Matte Sn	SnPb	
U41	TQFP-144	Matte Sn	SnPb	
U58	TQFP-144	Matte Sn	SnPb	
U03	TQFP-144	SnPb Dip	SnPb	
U31	TQFP-144	SnPb Dip	SnPb	
U34	TQFP-144	SnPb Dip	SnPb	
U48	TQFP-144	SnPb Dip	SnPb	
U57	TQFP-144	SnPb Dip	SnPb	
U12	TSOP-50	SnBi	SnPb	
U25	TSOP-50	SnBi	SnPb	
U29	TSOP-50	SnBi	SnPb	
U39	TSOP-50	SnBi	SnPb	
U61	TSOP-50	SnBi	SnPb	
U16	TSOP-50	SnPb	SnPb	
U24	TSOP-50	SnPb	SnPb	
U26	TSOP-50	SnPb	SnPb	
U40	TSOP-50	SnPb	SnPb	
U62	TSOP-50	SnPb	SnPb	

8.5.2 Assembly Details

- Reflow Soldering
- Location – BAE Systems Irving, Texas
- Reflow Profile = SnPb
 - Preheat = ~ 120 seconds @140-183°C
 - Solder joint peak temperature = 225°C
 - Time above reflow = 60-90 sec
 - Ramp Rate = 2-3 °C/sec
- Wave Soldering
- Location – BAE Systems Irving, Texas
- Wave Profile = SnPb
 - Solder Pot Temperature = 250°C
 - Preheat Board T = 101°C
 - Peak Temperature = 144°C
 - Speed: 110 cm/min

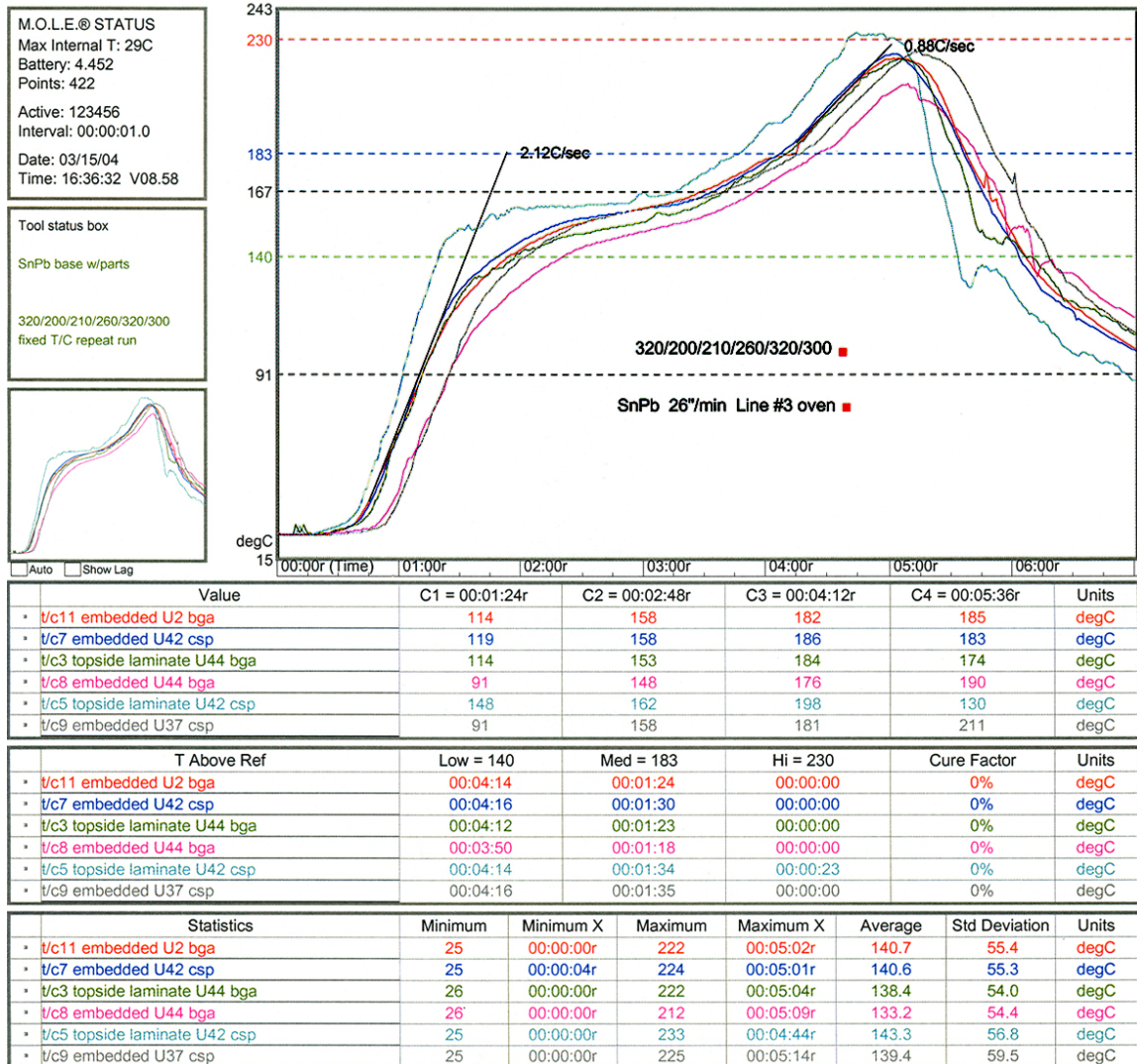


Figure 8 Example Reflow Oven Profile (SnPb)

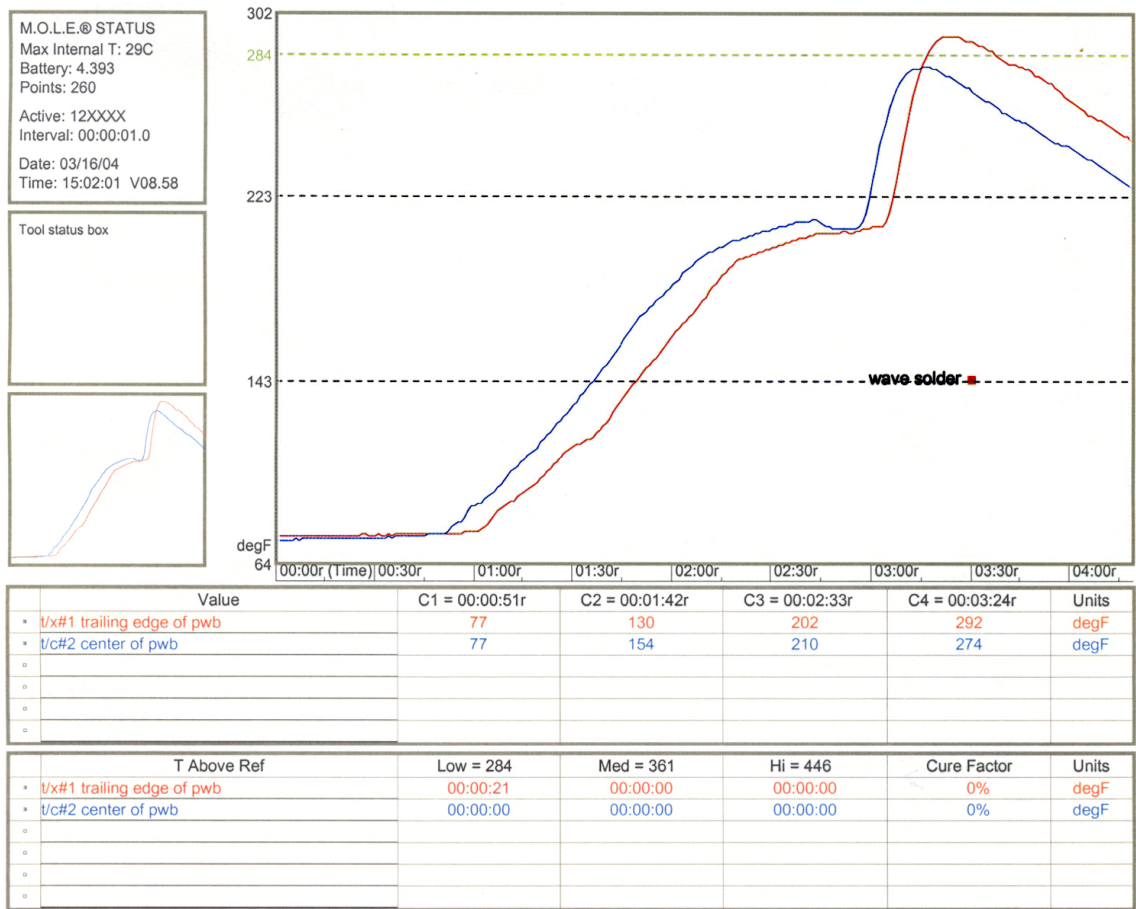


Figure 9 Example Wave Solder Profile (SnPb)

8.6 SnPb Manufactured ([Batch D](#))

8.6.1 Bare Boards

- 17 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 12 Test Vehicle Tracker – SnPb Manufactured Test Vehicles ([Batch D](#))

Project Activity	Board Number	Board Finish
Extra Boards	SN2	Immersion Ag
Test Vehicle Characterization	SN4	
Vibration	SN15	
	SN16	
	SN17	
	SN18	
	SN19	
Drop Testing	SN25	
	SN26	
	SN27	
	SN28	
	SN29	
Mechanical Shock	SN30	
	SN31	
	SN32	
	SN33	
	SN34	

Table 13 Component Finish Matrix – SnPb Manufactured Test Vehicles ([Batch D](#))

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U18	BGA-225	SnPb	SnPb	
U43	BGA-225	SnPb	SnPb	
U04	BGA-225	SnPb	SnPb	
U06	BGA-225	SnPb	SnPb	
U55	BGA-225	SnPb	SnPb	
U02	BGA-225	SnPb	SnPb	
U05	BGA-225	SnPb	SnPb	
U21	BGA-225	SnPb	SnPb	
U44	BGA-225	SnPb	SnPb	
U56	BGA-225	SnPb	SnPb	
U09	CLCC-20	SnPb	SnPb	
U13	CLCC-20	SnPb	SnPb	
U22	CLCC-20	SnPb	SnPb	
U46	CLCC-20	SnPb	SnPb	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U53	CLCC-20	SnPb	SnPb	
U10	CLCC-20	SnPb	SnPb	
U14	CLCC-20	SnPb	SnPb	
U17	CLCC-20	SnPb	SnPb	
U45	CLCC-20	SnPb	SnPb	
U52	CLCC-20	SnPb	SnPb	
U32	CSP-100	SnPb	SnPb	
U33	CSP-100	SnPb	SnPb	
U35	CSP-100	SnPb	SnPb	
U50	CSP-100	SnPb	SnPb	
U63	CSP-100	SnPb	SnPb	
U19	CSP-100	SnPb	SnPb	
U36	CSP-100	SnPb	SnPb	
U37	CSP-100	SnPb	SnPb	
U42	CSP-100	SnPb	SnPb	
U60	CSP-100	SnPb	SnPb	
U08	PDIP-20	SnPb		SnPb
U23	PDIP-20	SnPb		SnPb
U49	PDIP-20	SnPb		SnPb
U59	PDIP-20	SnPb		SnPb
U30	PDIP-20	SnPb		SnPb
U38	PDIP-20	SnPb		SnPb
U11	PDIP-20	SnPb		SnPb
U51	PDIP-20	SnPb		SnPb
U15	QFN	SnPb	SnPb	
U27	QFN	SnPb	SnPb	
U28	QFN	SnPb	SnPb	
U47	QFN	SnPb	SnPb	
U54	QFN	SnPb	SnPb	
U01	TQFP-144	Matte Sn	SnPb	
U07	TQFP-144	Matte Sn	SnPb	
U20	TQFP-144	Matte Sn	SnPb	
U41	TQFP-144	Matte Sn	SnPb	
U58	TQFP-144	Matte Sn	SnPb	
U03	TQFP-144	Matte Sn	SnPb	
U31	TQFP-144	Matte Sn	SnPb	
U34	TQFP-144	Matte Sn	SnPb	
U48	TQFP-144	Matte Sn	SnPb	
U57	TQFP-144	Matte Sn	SnPb	
U12	TSOP-50	SnPb	SnPb	
U25	TSOP-50	SnPb	SnPb	
U29	TSOP-50	SnPb	SnPb	
U39	TSOP-50	SnPb	SnPb	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U61	TSOP-50	SnPb	SnPb	
U16	TSOP-50	SnPb	SnPb	
U24	TSOP-50	SnPb	SnPb	
U26	TSOP-50	SnPb	SnPb	
U40	TSOP-50	SnPb	SnPb	
U62	TSOP-50	SnPb	SnPb	

8.6.2 Assembly Details

- Reflow Soldering
- Location – BAE Systems Irving, Texas
- Reflow Profile = SnPb
 - Preheat = ~ 120 seconds @ 140-183°C
 - Solder joint peak temperature = 225°C
 - Time above reflow = 60-90 sec
 - Ramp Rate = 2-3 °C/sec
- Wave Soldering
- Location – BAE Systems Irving, Texas
- Wave Profile = SnPb
 - Solder Pot Temperature = 250°C
 - Preheat Board T = 101°C
 - Peak Temperature = 144°C
 - Speed: 110 cm/min

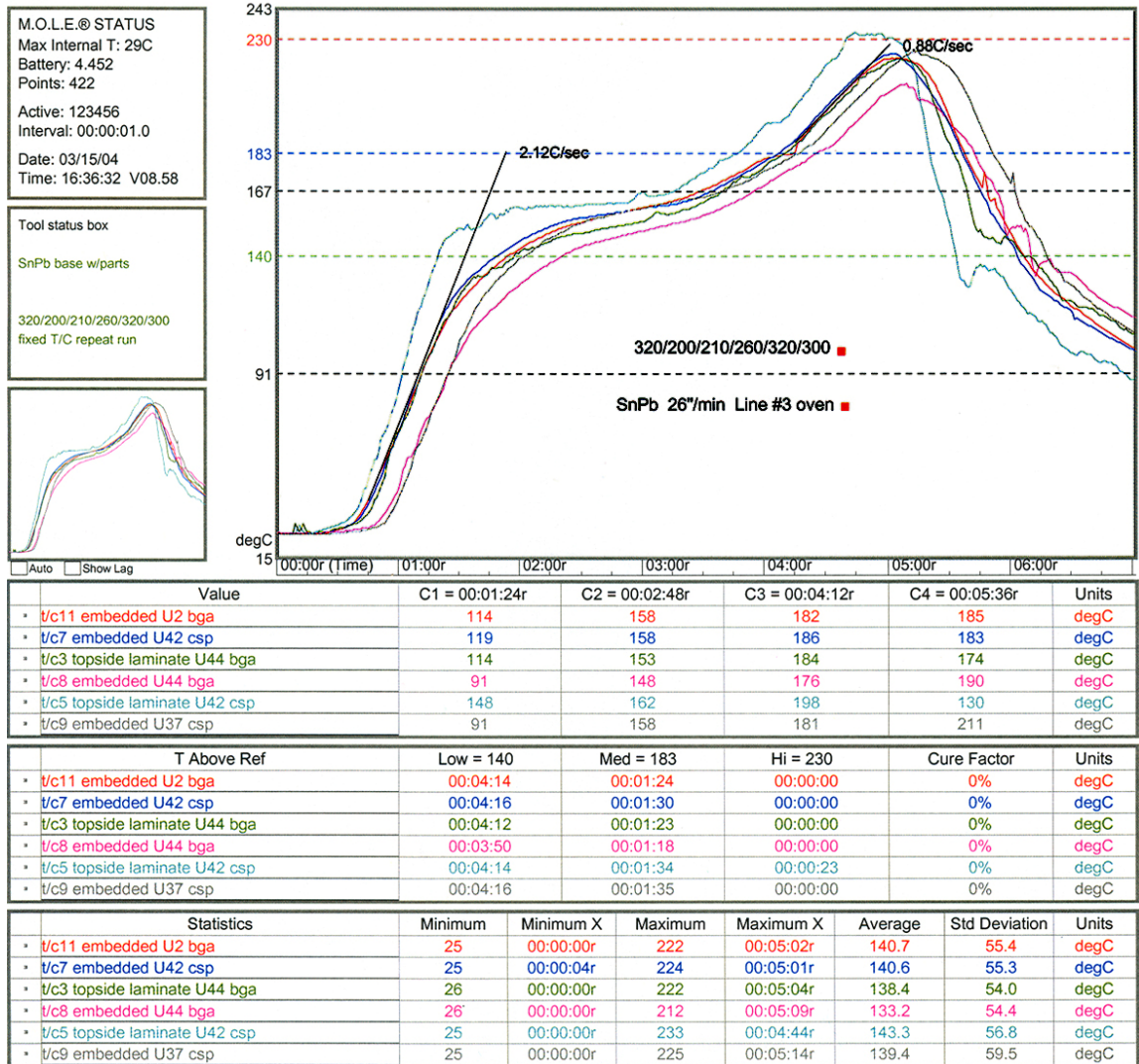


Figure 10 Example Reflow Oven Profile (SnPb)

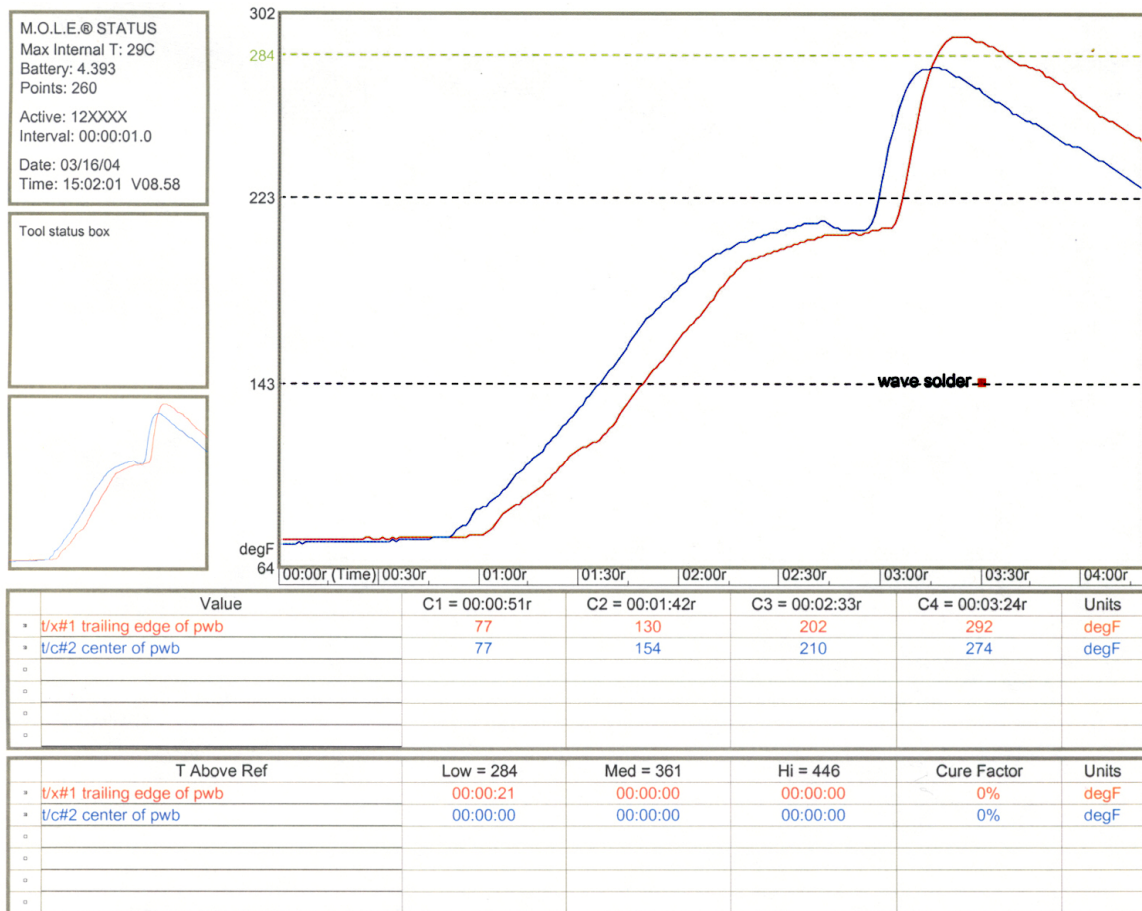


Figure 11 Example Wave Solder Profile (SnPb)

8.7 Lead-Free Manufactured ([Batch E](#))

8.7.1 Bare Boards

- 20 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag and ENIG surface finishes

Table 14 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles ([Batch E](#))

Project Activity	Board Number	Board Finish	Board Number	Board Finish
Extra Boards	SN35	Immersion Ag	N/A	ENIG
Test Vehicle Characterization	SN39		SN93	
Thermal Cycling: -55C to +125C	SN41		SN95	
	SN42			
	SN43			
	SN44			
	SN45			
Thermal Cycling: -20C to +80C	SN50		N/A	
	SN51			
	SN52			
	SN53			
	SN54			
Combined Environments Testing	SN69		SN97	
	SN70			
	SN71			
	SN72			
	SN73			

Table 15 Component Finish Matrix – Lead-Free Manufactured Test Vehicles ([Batch E](#))

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U02	BGA-225	SAC405	SAC305	
U05	BGA-225	SAC405	SAC305	
U21	BGA-225	SAC405	SAC305	
U44	BGA-225	SAC405	SAC305	
U56	BGA-225	SAC405	SAC305	
U18	BGA-225	SnPb	SAC305	
U43	BGA-225	SnPb	SAC305	
U04	BGA-225	SnPb	SAC305	
U06	BGA-225	SnPb	SAC305	
U55	BGA-225	SnPb	SAC305	
U10	CLCC-20	SAC305	SAC305	
U14	CLCC-20	SAC305	SAC305	
U17	CLCC-20	SAC305	SAC305	
U45	CLCC-20	SAC305	SAC305	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U52	CLCC-20	SAC305	SAC305	
U09	CLCC-20	SnPb	SAC305	
U13	CLCC-20	SnPb	SAC305	
U22	CLCC-20	SnPb	SAC305	
U46	CLCC-20	SnPb	SAC305	
U53	CLCC-20	SnPb	SAC305	
U19	CSP-100	SAC105	SAC305	
U36	CSP-100	SAC105	SAC305	
U37	CSP-100	SAC105	SAC305	
U42	CSP-100	SAC105	SAC305	
U60	CSP-100	SAC105	SAC305	
U32	CSP-100	SnPb	SAC305	
U33	CSP-100	SnPb	SAC305	
U35	CSP-100	SnPb	SAC305	
U50	CSP-100	SnPb	SAC305	
U63	CSP-100	SnPb	SAC305	
U08	PDIP-20	NiPdAu		SN100C
U23	PDIP-20	NiPdAu		SN100C
U49	PDIP-20	NiPdAu		SN100C
U59	PDIP-20	NiPdAu		SN100C
U11	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	Matte Sn	SAC305	
U27	QFN	Matte Sn	SAC305	
U28	QFN	Matte Sn	SAC305	
U47	QFN	Matte Sn	SAC305	
U54	QFN	Matte Sn	SAC305	
U03	TQFP-144	Matte Sn	SAC305	
U31	TQFP-144	Matte Sn	SAC305	
U34	TQFP-144	Matte Sn	SAC305	
U48	TQFP-144	Matte Sn	SAC305	
U57	TQFP-144	Matte Sn	SAC305	
U01	TQFP-144	SnPb Dip	SAC305	
U07	TQFP-144	SnPb Dip	SAC305	
U20	TQFP-144	SnPb Dip	SAC305	
U41	TQFP-144	SnPb Dip	SAC305	
U58	TQFP-144	SnPb Dip	SAC305	
U16	TSOP-50	SnBi	SAC305	
U24	TSOP-50	SnBi	SAC305	
U26	TSOP-50	SnBi	SAC305	
U40	TSOP-50	SnBi	SAC305	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U62	TSOP-50	SnBi	SAC305	
U12	TSOP-50	SnPb	SAC305	
U25	TSOP-50	SnPb	SAC305	
U29	TSOP-50	SnPb	SAC305	
U39	TSOP-50	SnPb	SAC305	
U61	TSOP-50	SnPb	SAC305	

8.7.2 Assembly Details

- Reflow Soldering
- Location – BAE Systems Irving, Texas
- Reflow Profile = SAC305
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Soldering
- Location – Scorpio Solutions
- Wave Profile = SN100C
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

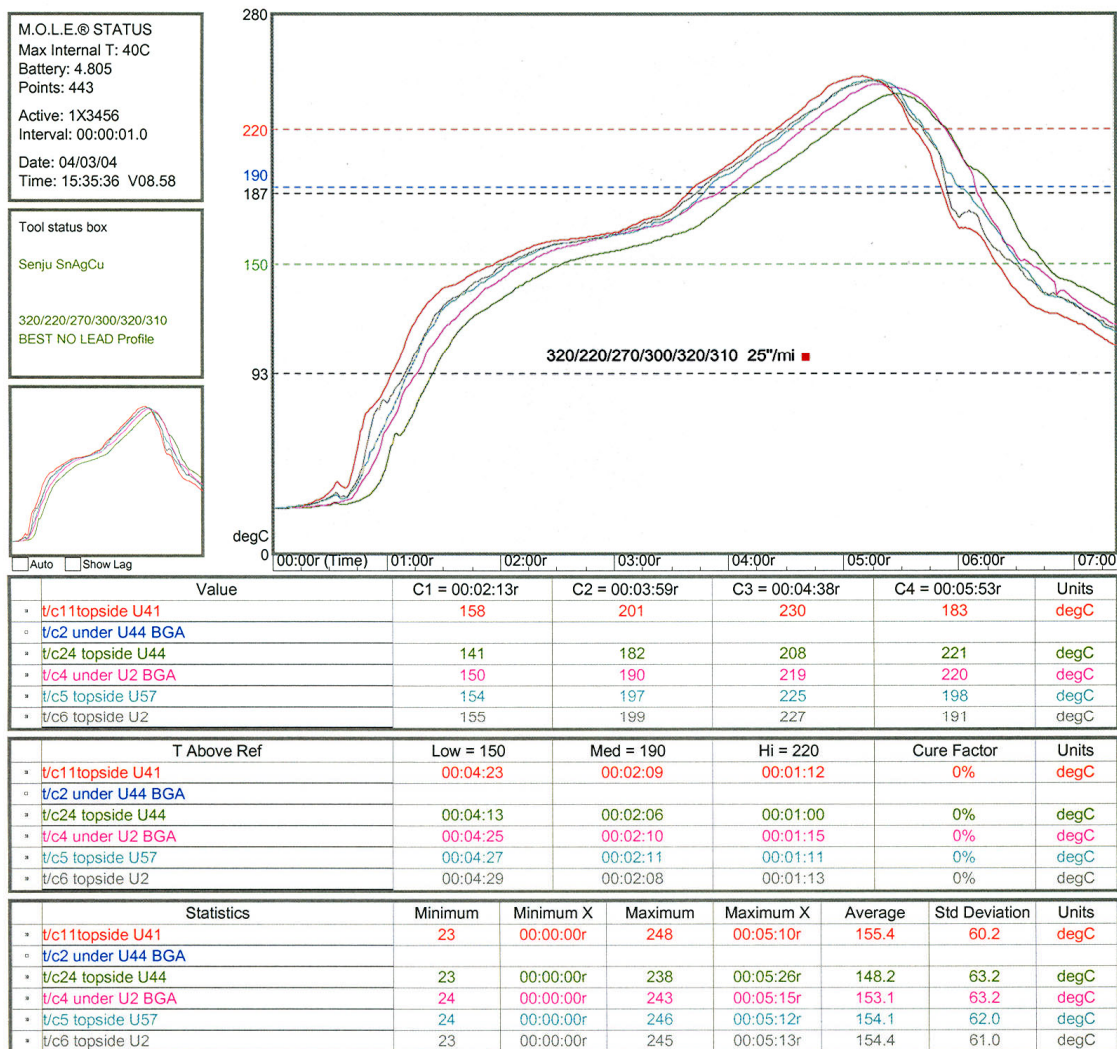
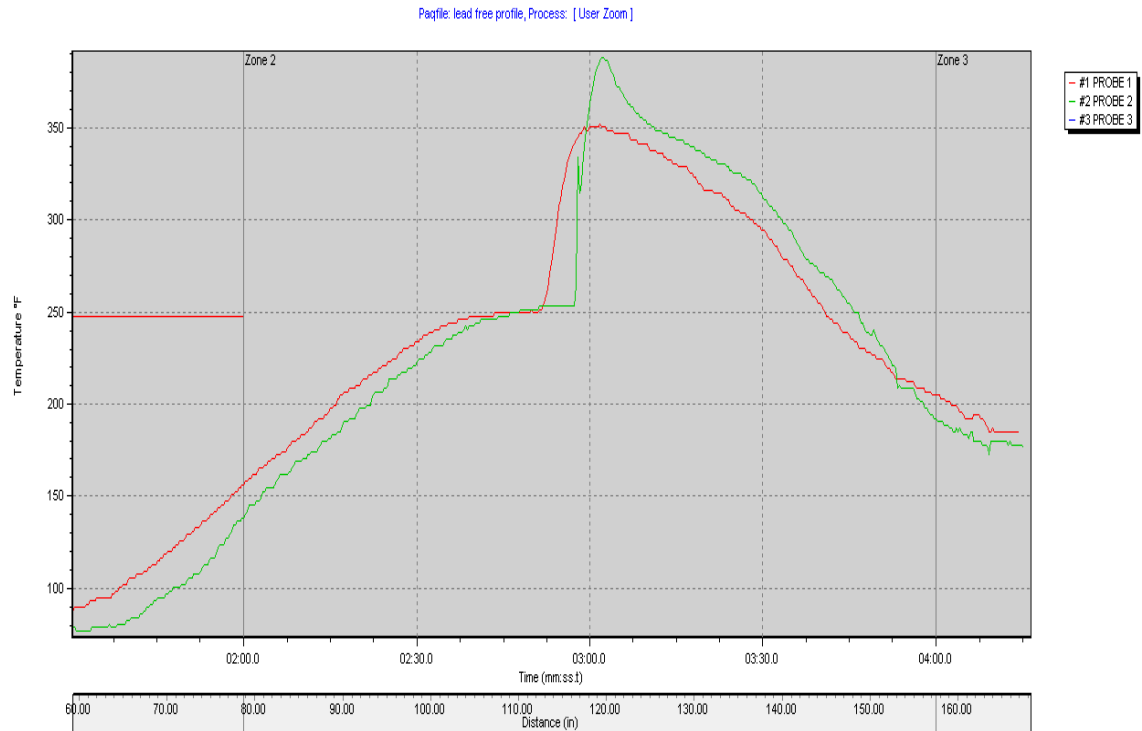


Figure 12 Example Reflow Oven Profile - Lead-Free (SAC305)



Reflow Results					
Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	xxx	xxx	00:00.0	xxx	

Figure 13 Example Wave Solder Profile - Lead-Free (SN100C)

8.8 Lead-Free Manufactured ([Batch F](#))

8.8.1 Bare Boards

- 43 boards
- 14.5"X 9"X 0.09"
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag and ENIG surface finishes

Table 16 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles ([Batch F](#))

Project Activity	Board Number	Board Finish	Board Number	Board Finish
Extra Boards	SN56	Immersion Ag	N/A	ENIG
Test Vehicle Characterization	SN58		SN94	
Vibration	SN36		SN96	
	SN40			
	SN57			
	SN76			
	SN78			
Drop Testing	SN55		N/A	
	SN59			
	SN74			
	SN75			
	SN77			
Mechanical Shock	SN88		N/A	
	SN89			
	SN90			
	SN91			
	SN92			
Boards for Crane Rework Effort				
Extra Boards	SN37	Immersion Ag		
	SN38			
Test Vehicle Characterization	N/A			
Thermal Cycling: -55C to +125C	SN46			
	SN47			
	SN48			
	SN49			
Thermal Cycling: -20C to +80C	N/A			
Vibration	SN60			
	SN61			
	SN62			
	SN63			
	SN64			
	SN65			
	SN66			
	SN67			
	SN68			
Combined Environments Testing	N/A			
Drop Testing	SN79			
	SN80			
	SN81			
	SN82			
	SN83			
	SN84			
	SN85			
	SN86			
	SN87			
Mechanical Shock	N/A			

Table 17 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch F)

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U18	BGA-225	SAC405	SAC305	
U43	BGA-225	SAC405	SAC305	
U04	BGA-225	SAC405	SAC305	
U06	BGA-225	SAC405	SAC305	
U55	BGA-225	SAC405	SAC305	
U02	BGA-225	SAC405	SAC305	
U05	BGA-225	SAC405	SAC305	
U21	BGA-225	SAC405	SAC305	
U44	BGA-225	SAC405	SAC305	
U56	BGA-225	SAC405	SAC305	
U09	CLCC-20	SAC305	SAC305	
U13	CLCC-20	SAC305	SAC305	
U22	CLCC-20	SAC305	SAC305	
U46	CLCC-20	SAC305	SAC305	
U53	CLCC-20	SAC305	SAC305	
U10	CLCC-20	SAC305	SAC305	
U14	CLCC-20	SAC305	SAC305	
U17	CLCC-20	SAC305	SAC305	
U45	CLCC-20	SAC305	SAC305	
U52	CLCC-20	SAC305	SAC305	
U32	CSP-100	SAC105	SAC305	
U33	CSP-100	SAC105	SAC305	
U35	CSP-100	SAC105	SAC305	
U50	CSP-100	SAC105	SAC305	
U63	CSP-100	SAC105	SAC305	
U19	CSP-100	SAC105	SAC305	
U36	CSP-100	SAC105	SAC305	
U37	CSP-100	SAC105	SAC305	
U42	CSP-100	SAC105	SAC305	
U60	CSP-100	SAC105	SAC305	
U08	PDIP-20	NiPdAu		SN100C
U23	PDIP-20	NiPdAu		SN100C
U49	PDIP-20	NiPdAu		SN100C
U59	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U11	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	Matte Sn	SAC305	
U27	QFN	Matte Sn	SAC305	
U28	QFN	Matte Sn	SAC305	
U47	QFN	Matte Sn	SAC305	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U54	QFN	Matte Sn	SAC305	
U01	TQFP-144	Matte Sn	SAC305	
U07	TQFP-144	Matte Sn	SAC305	
U20	TQFP-144	Matte Sn	SAC305	
U41	TQFP-144	Matte Sn	SAC305	
U58	TQFP-144	Matte Sn	SAC305	
U03	TQFP-144	Matte Sn	SAC305	
U31	TQFP-144	Matte Sn	SAC305	
U34	TQFP-144	Matte Sn	SAC305	
U48	TQFP-144	Matte Sn	SAC305	
U57	TQFP-144	Matte Sn	SAC305	
U12	TSOP-50	Sn	SAC305	
U25	TSOP-50	Sn	SAC305	
U29	TSOP-50	Sn	SAC305	
U39	TSOP-50	Sn	SAC305	
U61	TSOP-50	Sn	SAC305	
U16	TSOP-50	SnBi	SAC305	
U24	TSOP-50	SnBi	SAC305	
U26	TSOP-50	SnBi	SAC305	
U40	TSOP-50	SnBi	SAC305	
U62	TSOP-50	SnBi	SAC305	

8.8.2 Assembly Details

- Reflow Soldering
- Location – BAE Systems Irving, Texas
- Reflow Profile = SAC305:
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Soldering
- Location – Scorpio Solutions
- Wave Profile = SN100C:
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

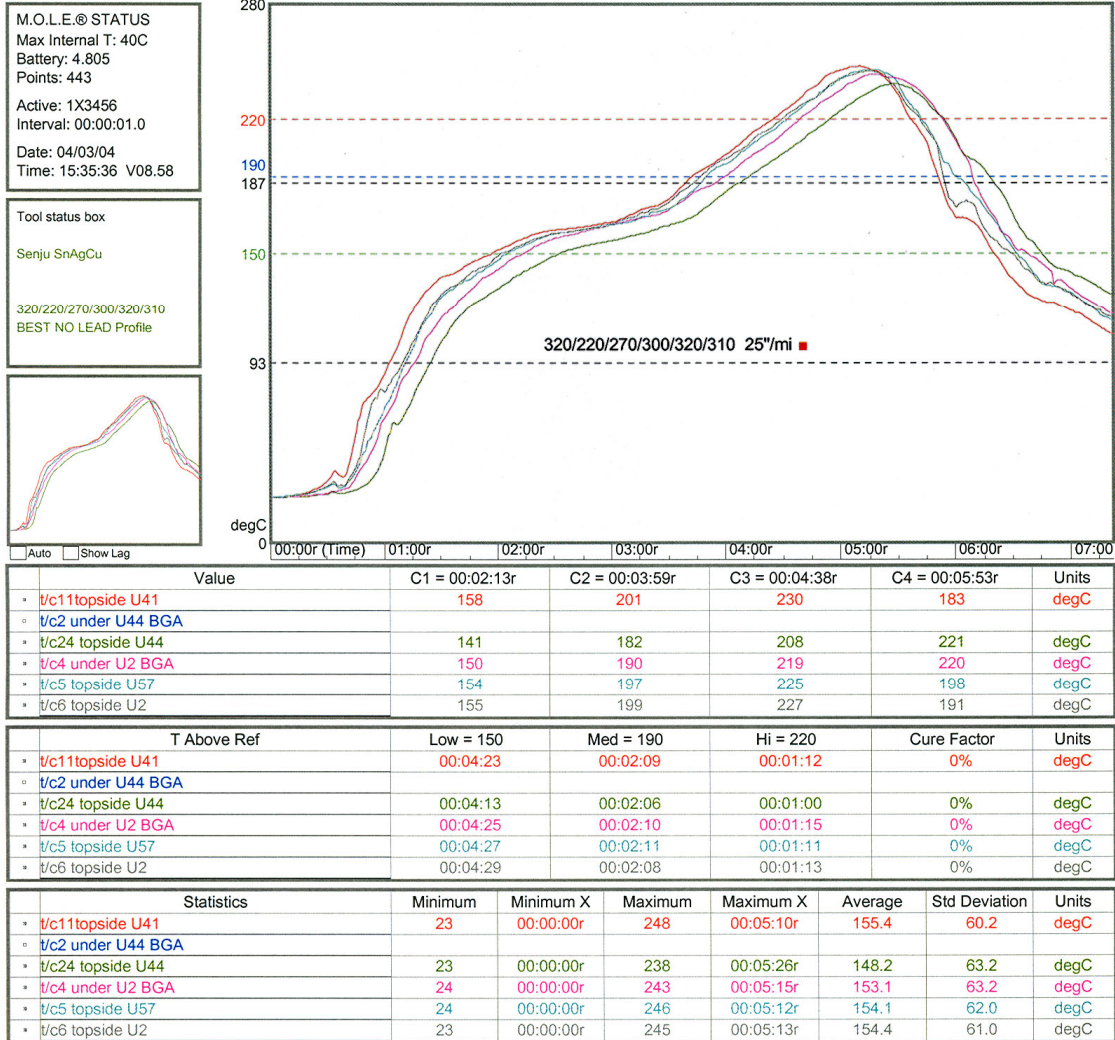
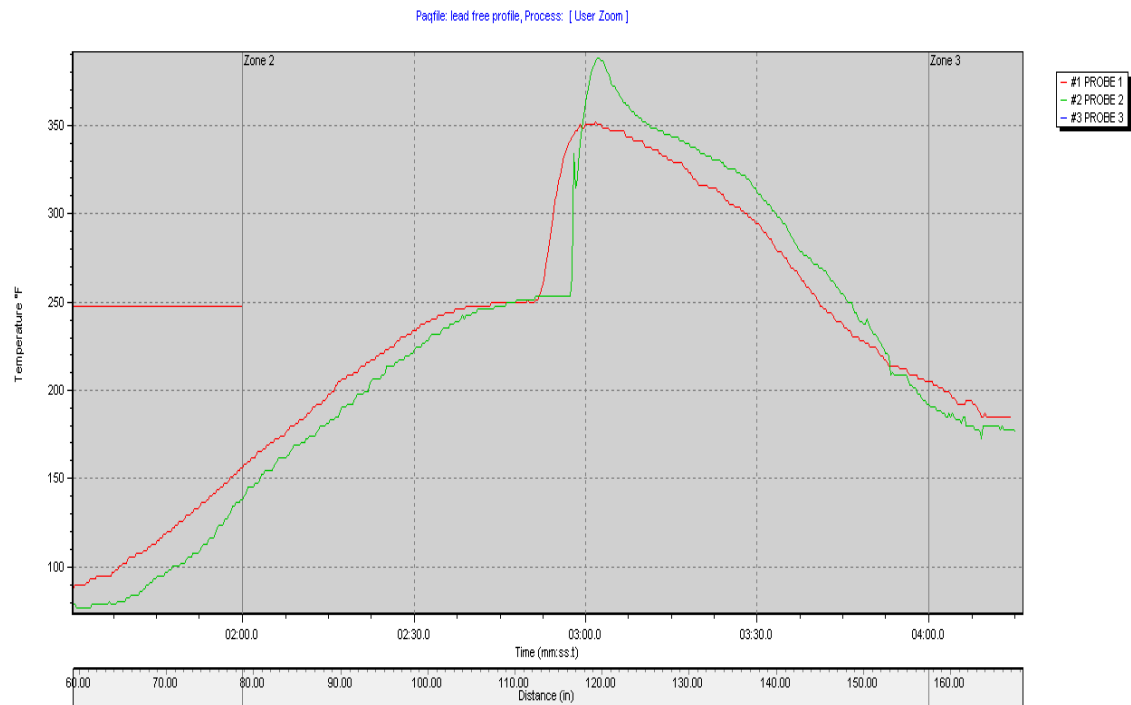


Figure 14 Example Reflow Oven Profile - Lead-Free (SAC305)



Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	***	***	00:00.0	***	

Figure 15 Example Wave Solder Profile - Lead-Free (SN100C)

8.9 Lead-Free Manufactured ([Batch G](#))

8.9.1 Bare Boards

- 11 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 18 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles ([Batch G](#))

Project Activity	Board Number	Board Finish
Extra Boards	--	Immersion Ag
Test Vehicle Characterization	SN100	
Thermal Cycling: -55C to +125C	SN102	
	SN103	
	SN104	
	SN105	
	SN106	
Thermal Cycling: -20C to +80C	--	
Combined Environments Testing	SN116	
	SN117	
	SN118	
	SN119	
	SN120	

Table 19 Component Finish Matrix – Lead-Free Manufactured Test Vehicles ([Batch G](#))

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U02	BGA-225	SAC405	SN100C	
U05	BGA-225	SAC405	SN100C	
U21	BGA-225	SAC405	SN100C	
U44	BGA-225	SAC405	SN100C	
U56	BGA-225	SAC405	SN100C	
U18	BGA-225	SnPb	SN100C	
U43	BGA-225	SnPb	SN100C	
U04	BGA-225	SnPb	SN100C	
U06	BGA-225	SnPb	SN100C	
U55	BGA-225	SnPb	SN100C	
U10	CLCC-20	SAC305	SN100C	
U14	CLCC-20	SAC305	SN100C	
U17	CLCC-20	SAC305	SN100C	
U45	CLCC-20	SAC305	SN100C	
U52	CLCC-20	SAC305	SN100C	
U09	CLCC-20	SnPb	SN100C	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U13	CLCC-20	SnPb	SN100C	
U22	CLCC-20	SnPb	SN100C	
U46	CLCC-20	SnPb	SN100C	
U53	CLCC-20	SnPb	SN100C	
U19	CSP-100	SAC105	SN100C	
U36	CSP-100	SAC105	SN100C	
U37	CSP-100	SAC105	SN100C	
U42	CSP-100	SAC105	SN100C	
U60	CSP-100	SAC105	SN100C	
U32	CSP-100	SnPb	SN100C	
U33	CSP-100	SnPb	SN100C	
U35	CSP-100	SnPb	SN100C	
U50	CSP-100	SnPb	SN100C	
U63	CSP-100	SnPb	SN100C	
U08	PDIP-20	NiPdAu		SN100C
U23	PDIP-20	NiPdAu		SN100C
U49	PDIP-20	NiPdAu		SN100C
U59	PDIP-20	NiPdAu		SN100C
U11	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	Matte Sn	SN100C	
U27	QFN	Matte Sn	SN100C	
U28	QFN	Matte Sn	SN100C	
U47	QFN	Matte Sn	SN100C	
U54	QFN	Matte Sn	SN100C	
U03	TQFP-144	Matte Sn	SN100C	
U31	TQFP-144	Matte Sn	SN100C	
U34	TQFP-144	Matte Sn	SN100C	
U48	TQFP-144	Matte Sn	SN100C	
U57	TQFP-144	Matte Sn	SN100C	
U01	TQFP-144	SnPb Dip	SN100C	
U07	TQFP-144	SnPb Dip	SN100C	
U20	TQFP-144	SnPb Dip	SN100C	
U41	TQFP-144	SnPb Dip	SN100C	
U58	TQFP-144	SnPb Dip	SN100C	
U16	TSOP-50	SnBi	SN100C	
U24	TSOP-50	SnBi	SN100C	
U26	TSOP-50	SnBi	SN100C	
U40	TSOP-50	SnBi	SN100C	
U62	TSOP-50	SnBi	SN100C	
U12	TSOP-50	SnPb	SN100C	

RefDes	Component	Component Finish	Reflow Solder Alloy	Wave Solder Alloy
U25	TSOP-50	SnPb	SN100C	
U29	TSOP-50	SnPb	SN100C	
U39	TSOP-50	SnPb	SN100C	
U61	TSOP-50	SnPb	SN100C	

8.9.2 Assembly Details

- Reflow Profile = SN100C
- Location – BAE Systems Irving, Texas
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Profile = SN100C
- Location – Scorpio Solutions
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

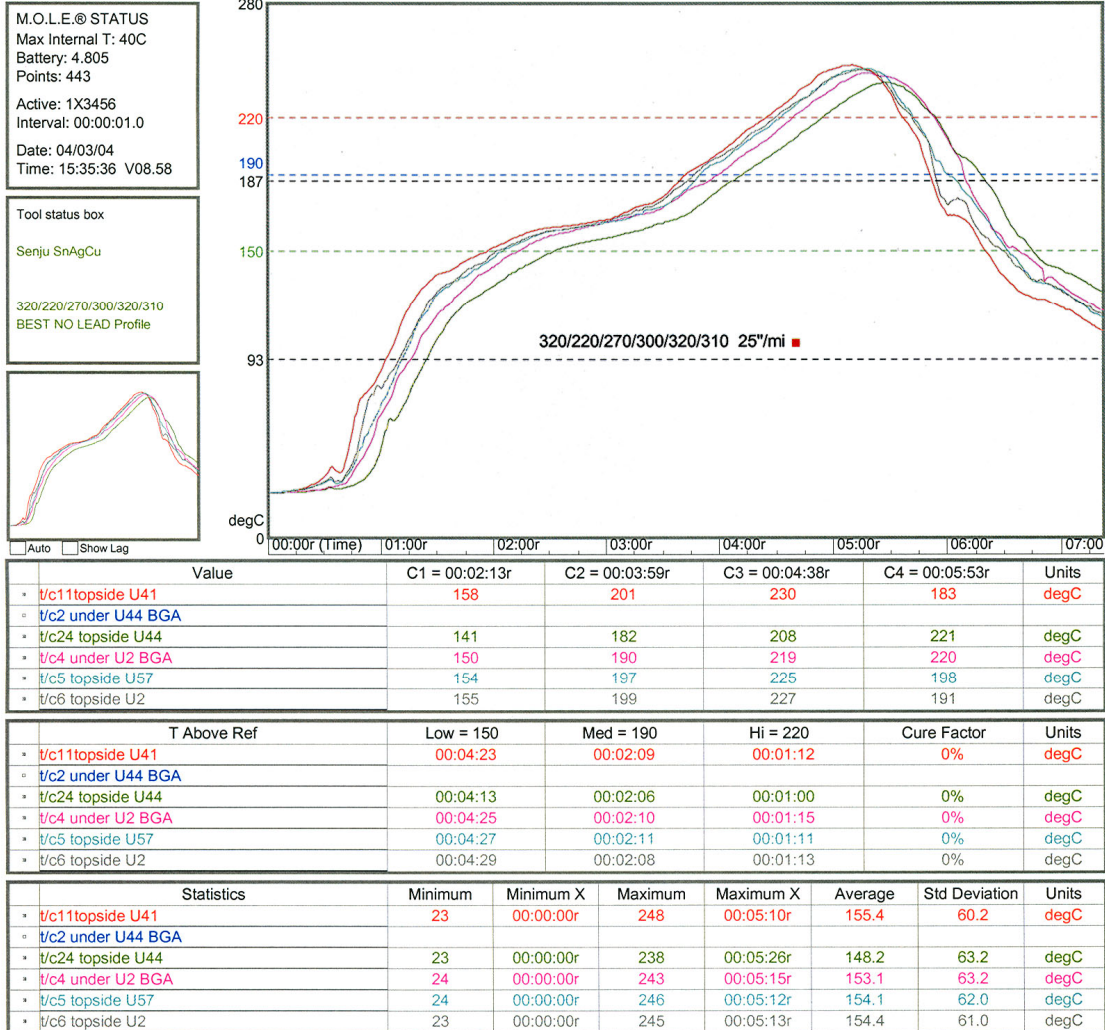
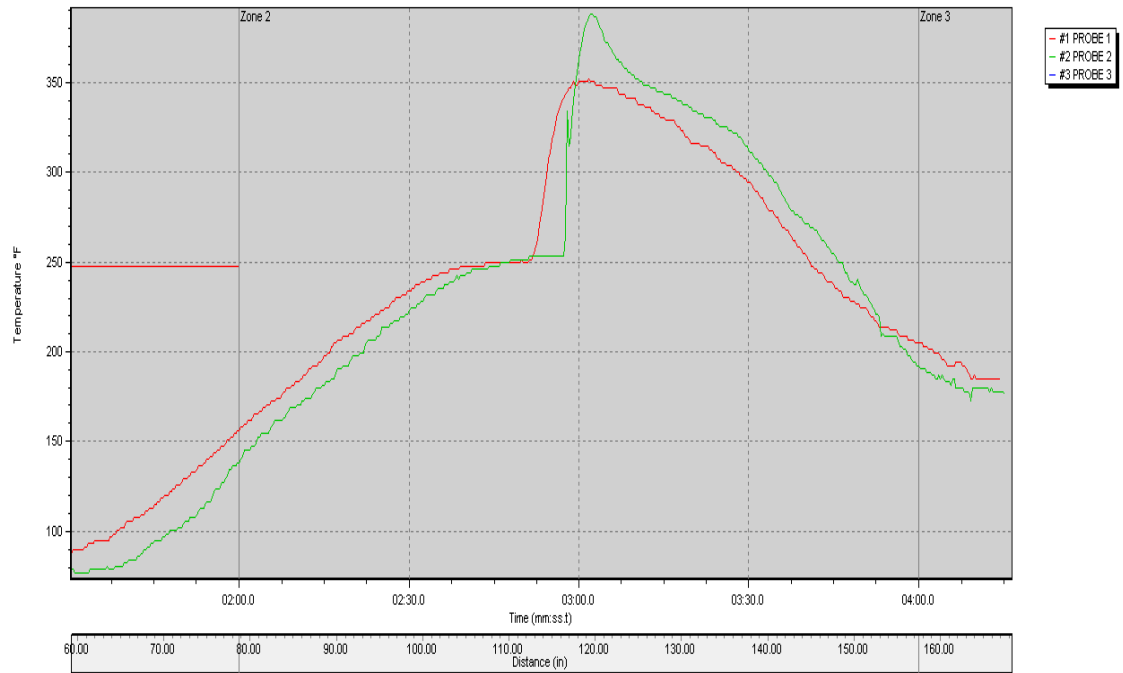


Figure 16 Example Reflow Oven Profile - Lead-Free (SN100C)

Pafile: lead free profile, Process: [User Zoom]



Reflow Results					
Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	***	***	00:00.0	***	

Figure 17 Example Wave Solder Profile - Lead-Free (SN100C)

8.10 Lead-Free Manufactured ([Batch H](#))

8.10.1 Bare Boards

- 6 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 20 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles ([Batch H](#))

Project Activity	Board Number	Board Finish
Extra Boards	--	Immersion Ag
Test Vehicle Characterization	SN101	
Vibration	SN111	
	SN112	
	SN113	
	SN114	
	SN115	
Drop Testing	--	
Mechanical Shock	--	

Table 21 Component Finish Matrix – Lead-Free Manufactured Test Vehicles ([Batch H](#))

RefDes	Component	Component Finish	Reflow Solder	Wave Solder
U18	BGA-225	SAC405	SN100C	
U43	BGA-225	SAC405	SN100C	
U04	BGA-225	SAC405	SN100C	
U06	BGA-225	SAC405	SN100C	
U55	BGA-225	SAC405	SN100C	
U02	BGA-225	SAC405	SN100C	
U05	BGA-225	SAC405	SN100C	
U21	BGA-225	SAC405	SN100C	
U44	BGA-225	SAC405	SN100C	
U56	BGA-225	SAC405	SN100C	
U09	CLCC-20	SAC305	SN100C	
U13	CLCC-20	SAC305	SN100C	
U22	CLCC-20	SAC305	SN100C	
U46	CLCC-20	SAC305	SN100C	
U53	CLCC-20	SAC305	SN100C	
U10	CLCC-20	SAC305	SN100C	
U14	CLCC-20	SAC305	SN100C	
U17	CLCC-20	SAC305	SN100C	
U45	CLCC-20	SAC305	SN100C	
U52	CLCC-20	SAC305	SN100C	

RefDes	Component	Component Finish	Reflow Solder	Wave Solder
U32	CSP-100	SAC105	SN100C	
U33	CSP-100	SAC105	SN100C	
U35	CSP-100	SAC105	SN100C	
U50	CSP-100	SAC105	SN100C	
U63	CSP-100	SAC105	SN100C	
U19	CSP-100	SAC105	SN100C	
U36	CSP-100	SAC105	SN100C	
U37	CSP-100	SAC105	SN100C	
U42	CSP-100	SAC105	SN100C	
U60	CSP-100	SAC105	SN100C	
U08	PDIP-20	NiPdAu		SN100C
U23	PDIP-20	NiPdAu		SN100C
U49	PDIP-20	NiPdAu		SN100C
U59	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U11	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	Matte Sn	SN100C	
U27	QFN	Matte Sn	SN100C	
U28	QFN	Matte Sn	SN100C	
U47	QFN	Matte Sn	SN100C	
U54	QFN	Matte Sn	SN100C	
U01	TQFP-144	Matte Sn	SN100C	
U07	TQFP-144	Matte Sn	SN100C	
U20	TQFP-144	Matte Sn	SN100C	
U41	TQFP-144	Matte Sn	SN100C	
U58	TQFP-144	Matte Sn	SN100C	
U03	TQFP-144	Matte Sn	SN100C	
U31	TQFP-144	Matte Sn	SN100C	
U34	TQFP-144	Matte Sn	SN100C	
U48	TQFP-144	Matte Sn	SN100C	
U57	TQFP-144	Matte Sn	SN100C	
U12	TSOP-50	Sn	SN100C	
U25	TSOP-50	Sn	SN100C	
U29	TSOP-50	Sn	SN100C	
U39	TSOP-50	Sn	SN100C	
U61	TSOP-50	Sn	SN100C	
U16	TSOP-50	SnBi	SN100C	
U24	TSOP-50	SnBi	SN100C	
U26	TSOP-50	SnBi	SN100C	
U40	TSOP-50	SnBi	SN100C	
U62	TSOP-50	SnBi	SN100C	

8.10.2 Assembly Details

- Reflow Profile = SN100C
- Location – BAE Systems Irving, Texas
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Profile = SN100C
- Location – Scorpio Solutions
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

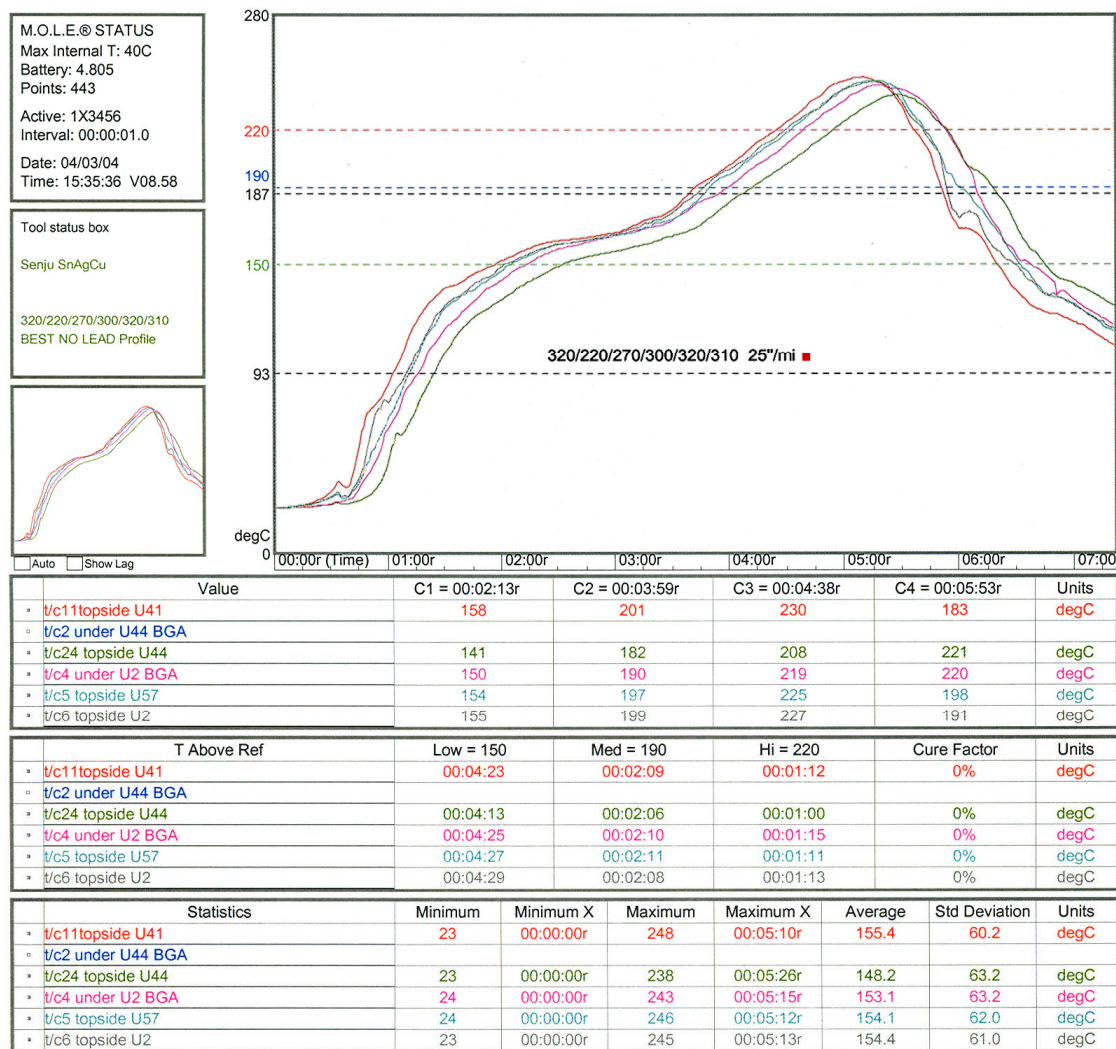
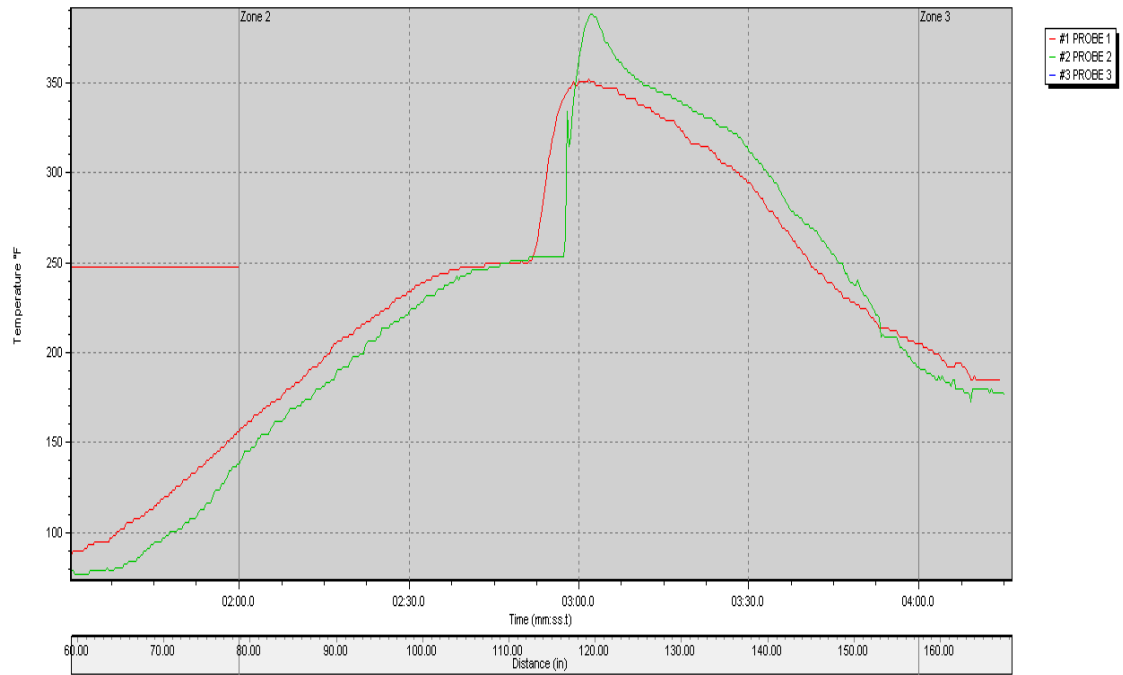


Figure 18 Example Reflow Oven Profile - Lead-Free (SN100C)

Paqfile: lead free profile, Process: [User Zoom]



Reflow Results					
Probe	Positive Slope (°F/sec)	Positive Slope Time (mm:ss.t)	Time Above Liquidus (361.4°F) (mm:ss.t)	Peak Temperature (°F)	Delta T (°F)
#1 (°F)	12.98	02:54.6	00:00.0	352.4	36.0
#2 (°F)	18.46	02:58.5	00:07.8	388.4	
#3 (°F)	***	***	00:00.0	***	

Figure 19 Example Wave Solder Profile - Lead-Free (SN100C)

8.11 Lead-Free Manufactured ([Batch I](#))

8.11.1 Bare Boards

- 6 boards
- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C
- Immersion Ag surface finish

Table 22 Test Vehicle Tracker - Lead-Free Manufactured Test Vehicles ([Batch I](#))

Project Activity	Board Number	Board Finish
Extra Boards	SN98	Immersion Ag
	SN99	
Test Vehicle Characterization	--	
	--	
Thermal Cycling: -55C to +125C	SN107	
	SN108	
	SN109	
	SN110	
Thermal Cycling: -20C to +80C	--	
	--	
Vibration	--	
Combined Environments Testing	--	
	--	
Drop Testing	--	
Mechanical Shock	--	

Table 23 Component Finish Matrix – Lead-Free Manufactured Test Vehicles ([Batch I](#))

RefDes	Component	Component Finish	Reflow Solder	Wave Solder
U18	BGA-225	SAC405	SN100C	
U43	BGA-225	SAC405	SN100C	
U04	BGA-225	SAC405	SN100C	
U06	BGA-225	SAC405	SN100C	
U55	BGA-225	SAC405	SN100C	
U02	BGA-225	SAC405	SN100C	
U05	BGA-225	SAC405	SN100C	
U21	BGA-225	SAC405	SN100C	
U44	BGA-225	SAC405	SN100C	
U56	BGA-225	SAC405	SN100C	
U09	CLCC-20	SAC305	SN100C	
U13	CLCC-20	SAC305	SN100C	
U22	CLCC-20	SAC305	SN100C	
U46	CLCC-20	SAC305	SN100C	
U53	CLCC-20	SAC305	SN100C	
U10	CLCC-20	SAC305	SN100C	

RefDes	Component	Component Finish	Reflow Solder	Wave Solder
U14	CLCC-20	SAC305	SN100C	
U17	CLCC-20	SAC305	SN100C	
U45	CLCC-20	SAC305	SN100C	
U52	CLCC-20	SAC305	SN100C	
U32	CSP-100	SN100C	SN100C	
U33	CSP-100	SN100C	SN100C	
U35	CSP-100	SN100C	SN100C	
U50	CSP-100	SN100C	SN100C	
U63	CSP-100	SN100C	SN100C	
U19	CSP-100	SN100C	SN100C	
U36	CSP-100	SN100C	SN100C	
U37	CSP-100	SN100C	SN100C	
U42	CSP-100	SN100C	SN100C	
U60	CSP-100	SN100C	SN100C	
U08	PDIP-20	NiPdAu		SN100C
U23	PDIP-20	NiPdAu		SN100C
U49	PDIP-20	NiPdAu		SN100C
U59	PDIP-20	Sn		SN100C
U30	PDIP-20	Sn		SN100C
U38	PDIP-20	Sn		SN100C
U11	PDIP-20	Sn		SN100C
U51	PDIP-20	Sn		SN100C
U15	QFN	Matte Sn	SN100C	
U27	QFN	Matte Sn	SN100C	
U28	QFN	Matte Sn	SN100C	
U47	QFN	Matte Sn	SN100C	
U54	QFN	Matte Sn	SN100C	
U01	TQFP-144	Matte Sn	SN100C	
U07	TQFP-144	Matte Sn	SN100C	
U20	TQFP-144	Matte Sn	SN100C	
U41	TQFP-144	Matte Sn	SN100C	
U58	TQFP-144	Matte Sn	SN100C	
U03	TQFP-144	Matte Sn	SN100C	
U31	TQFP-144	Matte Sn	SN100C	
U34	TQFP-144	Matte Sn	SN100C	
U48	TQFP-144	Matte Sn	SN100C	
U57	TQFP-144	Matte Sn	SN100C	
U12	TSOP-50	Sn	SN100C	
U25	TSOP-50	Sn	SN100C	
U29	TSOP-50	Sn	SN100C	
U39	TSOP-50	Sn	SN100C	
U61	TSOP-50	Sn	SN100C	
U16	TSOP-50	SnBi	SN100C	

RefDes	Component	Component Finish	Reflow Solder	Wave Solder
U24	TSOP-50	SnBi	SN100C	
U26	TSOP-50	SnBi	SN100C	
U40	TSOP-50	SnBi	SN100C	
U62	TSOP-50	SnBi	SN100C	

For Batch I only, the CSP components were re-balled by Premier Semiconductor Services. The original solder ball alloy was SAC105, Premier Semiconductor Services re-balled the components using SN100C solder balls.

8.11.2 Assembly Details

- Reflow Profile = SN100C
- Location – BAE Systems Irving, Texas
 - Preheat = 60-120 seconds @ 150-190°C
 - Peak temperature target = 243°C
 - Reflow: ~20 seconds above 230°C
 - ~30-90 seconds above 220°C
- Wave Profile = SN100C
- Location – Scorpio Solutions
 - Solder Pot Temperature = 265°C
 - Preheat Board T = 134°C
 - Peak Temperature = 157°C
 - Speed: 90 cm/min

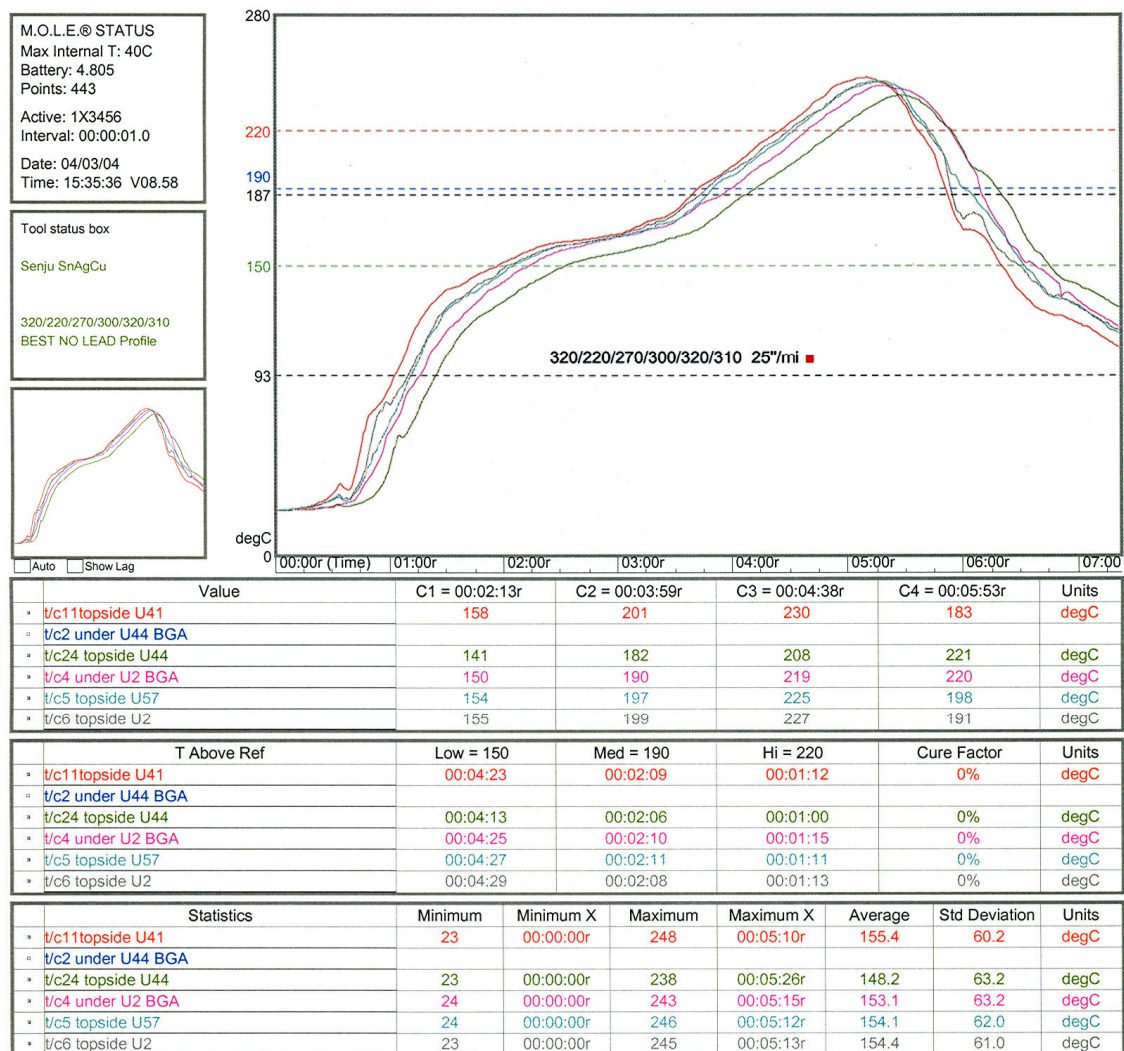


Figure 20 Example Reflow Oven Profile - Lead-Free (SN100C)

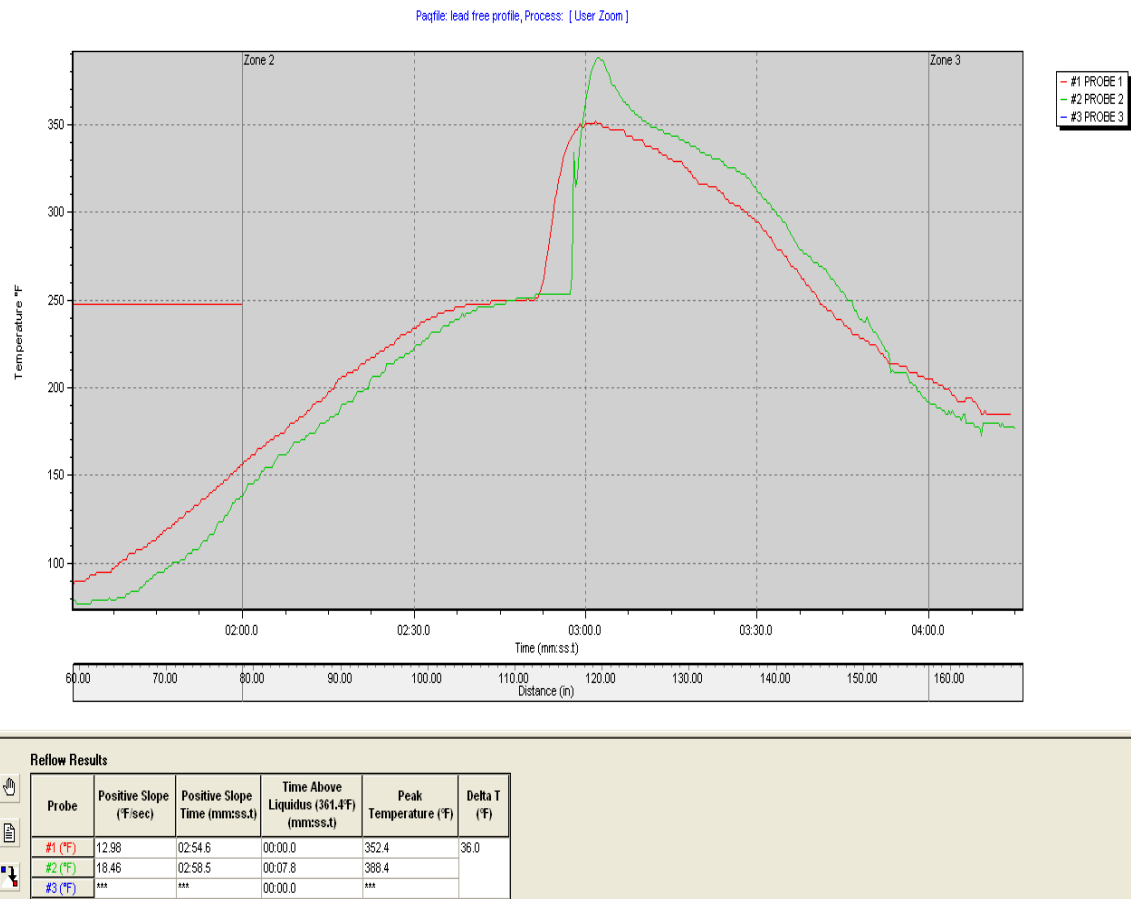


Figure 21 Example Wave Solder Profile - Lead-Free (SN100C)

9.0 Area Array X-Ray Analysis

Once test vehicle assembly is completed, all test vehicles will be shipped to Lockheed Martin for x-ray analysis of the area array components, BGA and CSP. The QFN components will also be analyzed. Percentage of voiding as well as ball shape will be documented. Appendix F provides the details for the x-ray analysis.

10.0 Manufactured Test Vehicle Characterization

Rockwell Collins will cross-section the manufactured test vehicles set aside for characterization. A minimum of 1 component from each component type will be cross sectioned.

Table 24 Manufactured Test Vehicles for Characterization

Project Activity	Batch / Board Number
Test Vehicle Characterization	Batch C / SN3
	Batch D / SN4
	Batch E / SN39
	Batch E / SN93
	Batch F / SN40
	Batch F / SN94
	Batch G / SN100
	Batch H / SN101

11.0 Rework Protocol

There is a large volume of rework being conducted for this project. In order to get the rework procedures completed in a timely manner, multiple facilities will be performing the rework activities. The following tables shows which test vehicles will be going to which facilities for rework:

Table 25 Rework Test Vehicles for BAE Systems

Project Activity	Batch / Board Number
Extra Boards	Batch A / SN161
	Batch A / SN162
	Batch B / SN121
	Batch B / SN122
Test Vehicle Characterization	Batch A / SN163
	Batch B / SN123
	Batch B / SN154
Vibration	Batch A / SN174
	Batch A / SN175
	Batch A / SN176
	Batch A / SN177
	Batch A / SN178
	Batch B / SN134
	Batch B / SN135
	Batch B / SN136
	Batch B / SN137
	Batch B / SN138
	Batch B / SN157
Combined Environments Testing	Batch A / SN179
	Batch A / SN180
	Batch A / SN181
	Batch A / SN182
	Batch A / SN183
	Batch B / SN139
	Batch B / SN140
	Batch B / SN141
	Batch B / SN142
	Batch B / SN143
	Batch B / SN158

Table 26 Rework Test Vehicles for Lockheed Martin

Project Activity	Batch / Board Number
Thermal Cycling: -55C to +125C	Batch A / SN164
	Batch A / SN165
	Batch A / SN166
	Batch A / SN167
	Batch A / SN168
	Batch B / SN124
	Batch B / SN125
	Batch B / SN126
	Batch B / SN127
	Batch B / SN128
	Batch B / SN155
Thermal Cycling: -20C to +80C	Batch A / SN169
	Batch A / SN170
	Batch A / SN171
	Batch A / SN172
	Batch A / SN173
	Batch B / SN129
	Batch B / SN130
	Batch B / SN131
	Batch B / SN132
	Batch B / SN133
	Batch B / SN156

Table 27 Rework Test Vehicles for Rockwell Collins

Project Activity	Batch / Board Number
Drop Testing	Batch A / SN184
	Batch A / SN185
	Batch A / SN186
	Batch A / SN187
	Batch A / SN188
	Batch B / SN144
	Batch B / SN145
	Batch B / SN146
	Batch B / SN147
	Batch B / SN148
	Batch B / SN159
Mechanical Shock	Batch A / SN189
	Batch A / SN190
	Batch A / SN191
	Batch A / SN192
	Batch A / SN193
	Batch B / SN149
	Batch B / SN150
	Batch B / SN151
	Batch B / SN152
	Batch B / SN153
	Batch B / SN160

Table 28 Component Finish Matrix – Lead-Free Rework (Batch A)

RefDes	Component	Original Component Finish	Reflow Solder	Wave Solder	New Component Finish	Rework Solder	Rework Profile
U18	BGA-225	SAC405	SAC305		SAC405	SnPb	Lead-Free
U43	BGA-225	SAC405	SAC305		SAC405	SnPb	
U06	BGA-225	SAC405	SAC305		SAC405	SnPb	
U02	BGA-225	SAC405	SAC305		SAC405	Flux Only	
U21	BGA-225	SAC405	SAC305		SAC405	Flux Only	
U56	BGA-225	SAC405	SAC305		SAC405	Flux Only	
U33	CSP-100	SAC105	SAC305		SAC105	SnPb	
U50	CSP-100	SAC105	SAC305		SAC105	Flux Only	
U19	CSP-100	SAC105	SAC305		SAC105	Flux Only	
U37	CSP-100	SAC105	SAC305		SAC105	Flux Only	
U42	CSP-100	SAC105	SAC305		SAC105	SnPb	
U60	CSP-100	SAC105	SAC305		SAC105	SnPb	
U11	PDIP-20	Sn		SN100C	Sn	SN100C	
U51	PDIP-20	Sn		SN100C	Sn	SN100C	
U12	TSOP-50	Sn	SAC305		Sn	SnPb	
U25	TSOP-50	Sn	SAC305		Sn	SnPb	
U24	TSOP-50	SnBi	SAC305		SnBi	SAC305	
U26	TSOP-50	SnBi	SAC305		SnBi	SAC305	

Table 29 Component Finish Matrix – SnPb Rework (Batch B)

RefDes	Component	Original Component Finish	Reflow Solder	Wave Solder	New Component Finish	Rework Solder	Rework Profile
U18	BGA-225	SnPb	SnPb		SAC405	SnPb	SnPb
U43	BGA-225	SnPb	SnPb		SAC405	SnPb	
U06	BGA-225	SnPb	SnPb		SAC405	SnPb	
U02	BGA-225	SnPb	SnPb		SnPb	Flux Only	
U21	BGA-225	SnPb	SnPb		SnPb	Flux Only	
U56	BGA-225	SnPb	SnPb		SnPb	Flux Only	
U33	CSP-100	SnPb	SnPb		SAC105	SnPb	
U50	CSP-100	SnPb	SnPb		SnPb	Flux Only	
U19	CSP-100	SnPb	SnPb		SnPb	Flux Only	
U37	CSP-100	SnPb	SnPb		SnPb	Flux Only	
U42	CSP-100	SnPb	SnPb		SAC105	SnPb	
U60	CSP-100	SnPb	SnPb		SAC105	SnPb	
U11	PDIP-20	SnPb		SnPb	Sn	SnPb	
U51	PDIP-20	SnPb		SnPb	Sn	SnPb	
U12	TSOP-50	SnPb	SnPb		SnPb	SnPb	
U25	TSOP-50	SnPb	SnPb		SnPb	SnPb	
U24	TSOP-50	SnPb	SnPb		Sn	SnPb	
U26	TSOP-50	SnPb	SnPb		Sn	SnPb	

Components being reworked have been grouped by rework solder alloy / material (SnPb, Flux only, SAC305 and SN100C). The location performing the rework can choose what order to rework the solder alloy / material groups, but must use the numbered order below for specific component locations within the solder alloy / material group. When reworking a component, the component is to be removed and replaced before moving to the next component.

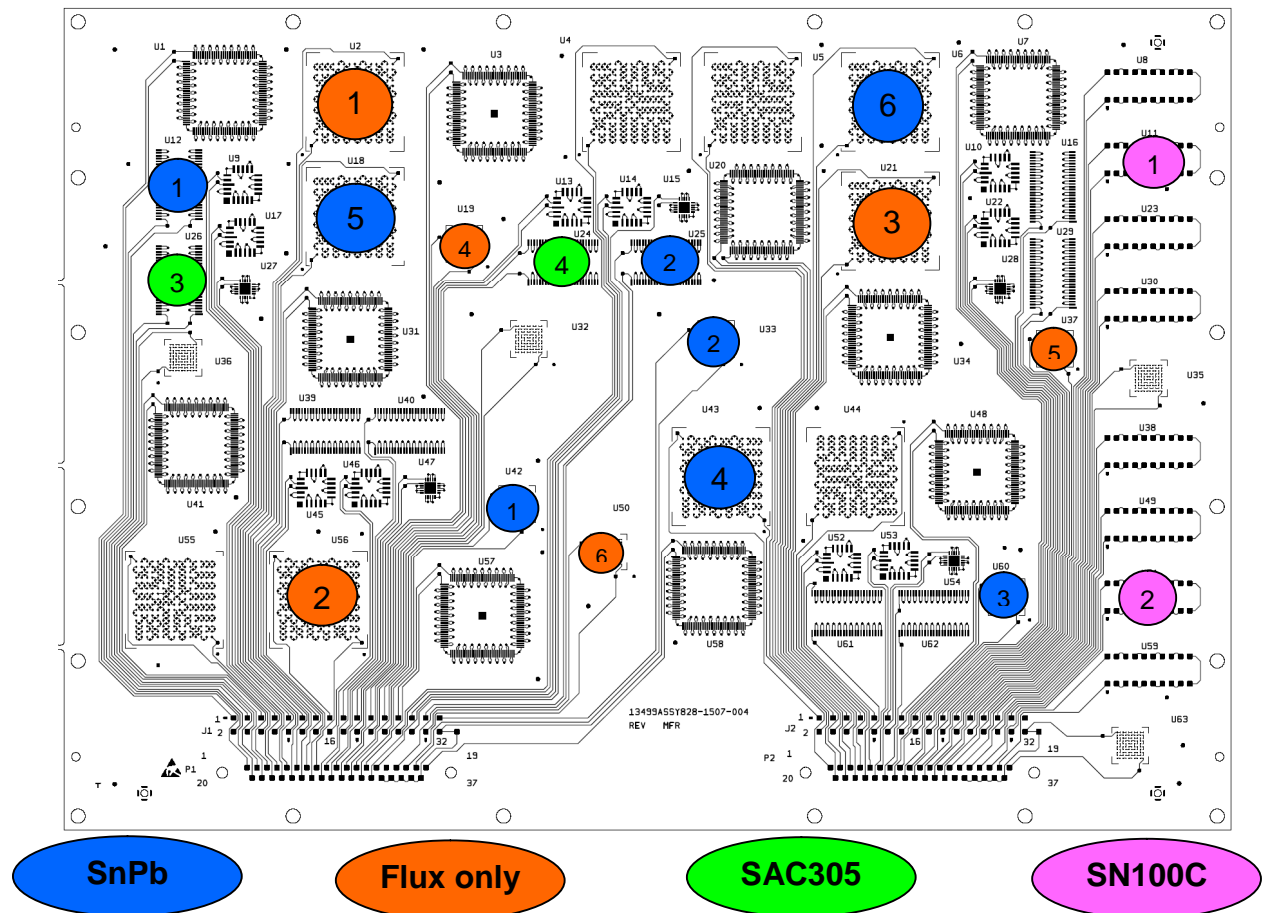


Figure 22 Rework Order = Batch A

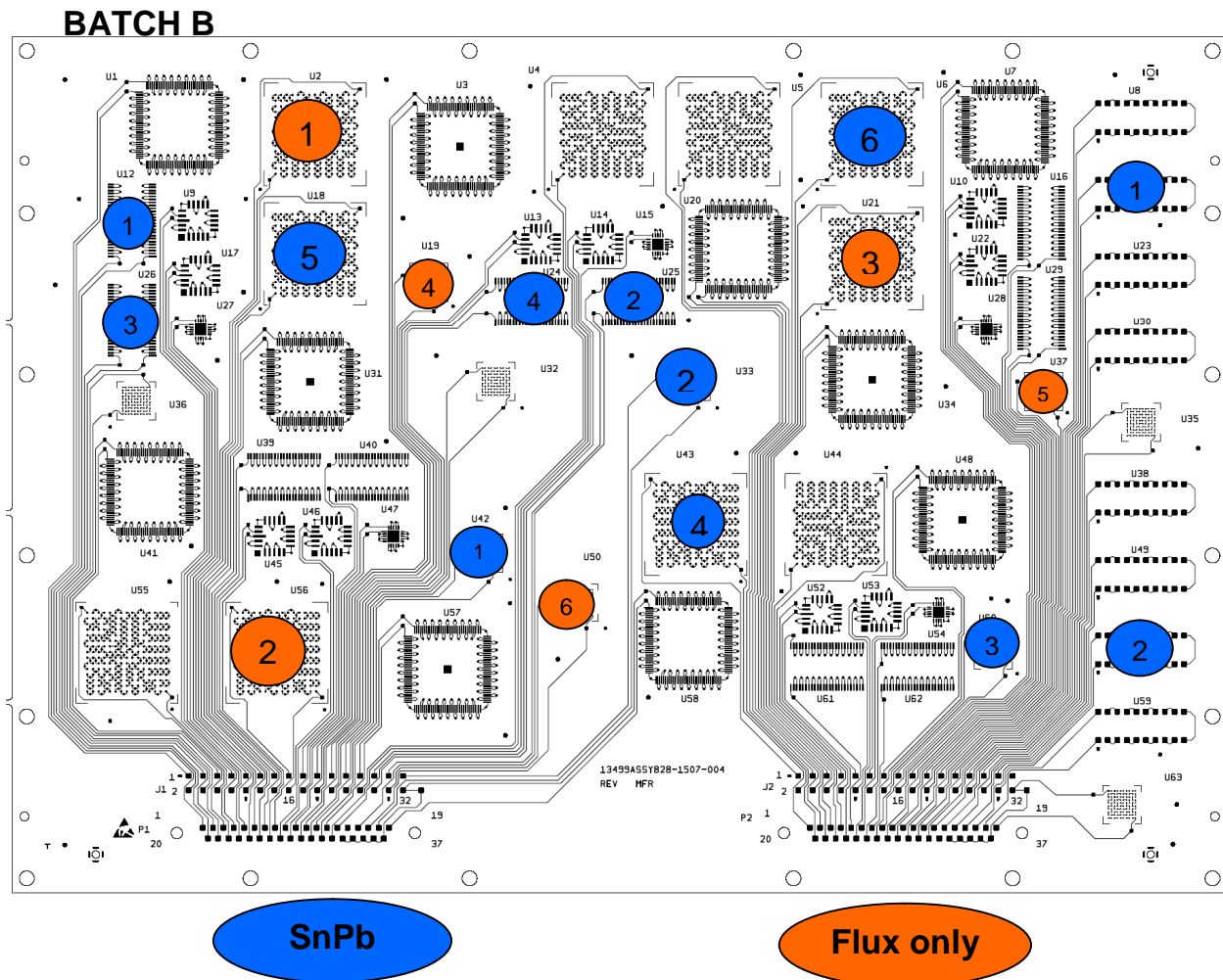


Figure 23 - Rework Order = Batch B

NOTE:

- Contamination: Please note that care needs to be taken not to contaminate the rework station being used for SnPb and lead-free rework procedures. Cross contamination can cause decreased reliability of solder interconnects.
- Flux: In any solder removal/replacement sequence, use of external flux (ROLO) is allowed.
- Repair: If needed, repairs can be made during rework. Each location will document any repairs needed.
- BGA rework: Solder paste will be applied to the BGA not the board.
- CSP rework: Solder paste will be applied to the CSP not the board.
- Rework Sequence: For all component types:
 - Remove component
 - Cool
 - Replace

11.1 Component Preparation

11.1.1 Moisture bake out per J-STD-033, table 4-1

- Prior to rework, bake the components for 48 hours @ 125°C

11.2 Rework Procedure per IPC-7711

11.2.1 Moisture bake out

- Prior to rework, bake boards for 4 hours @ 230°F and store in a dry environment until all rework is complete.

11.2.2 Cleaning

- In-line clean after rework (wash within shift), document multiple cleanings on traveler
- Clean as required per J-STD-001
- Document cleaning chemistry per rework location

11.2.3 Removal and Replacement

11.2.3.1 Removal of Leaded Through Hole Parts

- Remove components per IPC-7711 method 3.1.1

11.2.3.2 Replacement of Leaded Through Hole Parts

- Per J-STD 001 certified soldering
- Use Metcal STTC-138, 700°F tips and rosin base flux

11.2.3.3 Removal and Replacement of Leaded Surface Mount Devices

- Remove using solder wick and replace per J-STD 001
- Hand procedure per IPC 7711
 - Remove by using soldering iron method by removing excess solder using solder braid (wick). Heat and lift each lead from the pad surface using a dental pick or similar device.

11.2.3.4 Replacement of Leaded Surface Mount Devices

- Per J-STD 001 certified soldering
- Use Metcal STTC-125 or STTC-142, 700°F tips and rosin base flux

11.2.3.5 Removal and Replacement of area array components

- Removal per procedure IPC-7711 - 3.9.1
- Replace per procedure IPC-7711 - 5.7.2; use paste / tacky flux
- Thermal couple map
- Drill center and polarity corner to place thermal couple in every BGA, name profile using ref designator for SnPb and lead-free
 - .032"drill bit with a .090" depth.

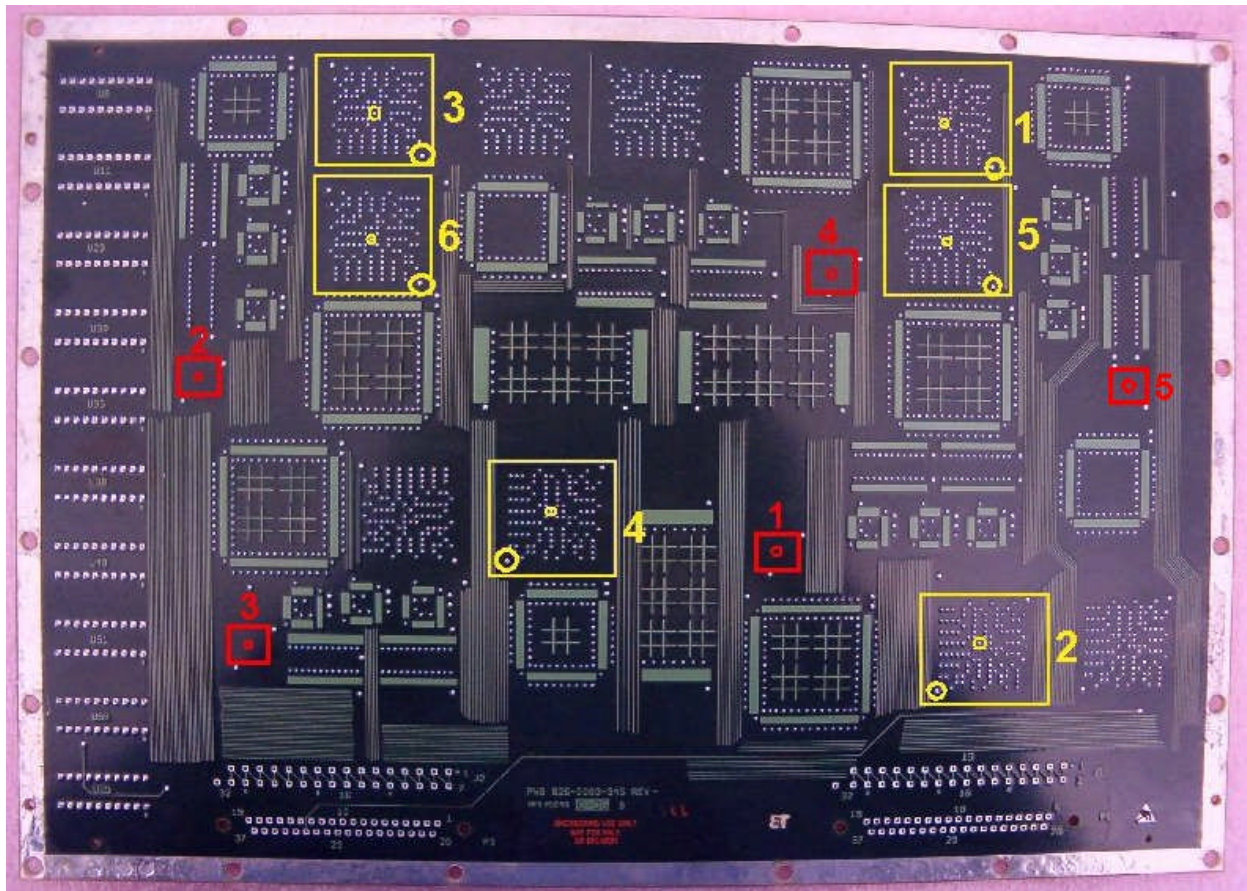


Figure 24 Thermal Couple Map, Bottom Side of the Test Vehicle**

** A JCAA/JGPP test vehicle was used for the thermal couple map since this work was done prior to the NASA-DoD test vehicles being available

- Tape off all areas around the component being reworked
- Hot air rework station with nitrogen per IPC-7711 3.9.1
 - Use regular or tacky flux, document type of flux
 - Nozzle table
 - Mini stencil
 - All 6 mil thick
 - Stainless steel
 - Laser cut
 - BGA = Standard mini stencil with 10% reduction
 - CSP = Standard mini stencil with 10% reduction

- **SnPb rework profile for area array removal and replacement**
 - Device joint target = 210°C +/- 5°C
 - Device top max target = 250°C
 - Board max = as measured by the board trigger thermal couple; will be recorded
 - Reflow:
 - ~60 - 120 seconds @ 140-180 °C
 - ~60 - 120 seconds above 183 °C
 - Delta T from center to corner ball = 10°C
 - Ramp rate = <4°C/sec

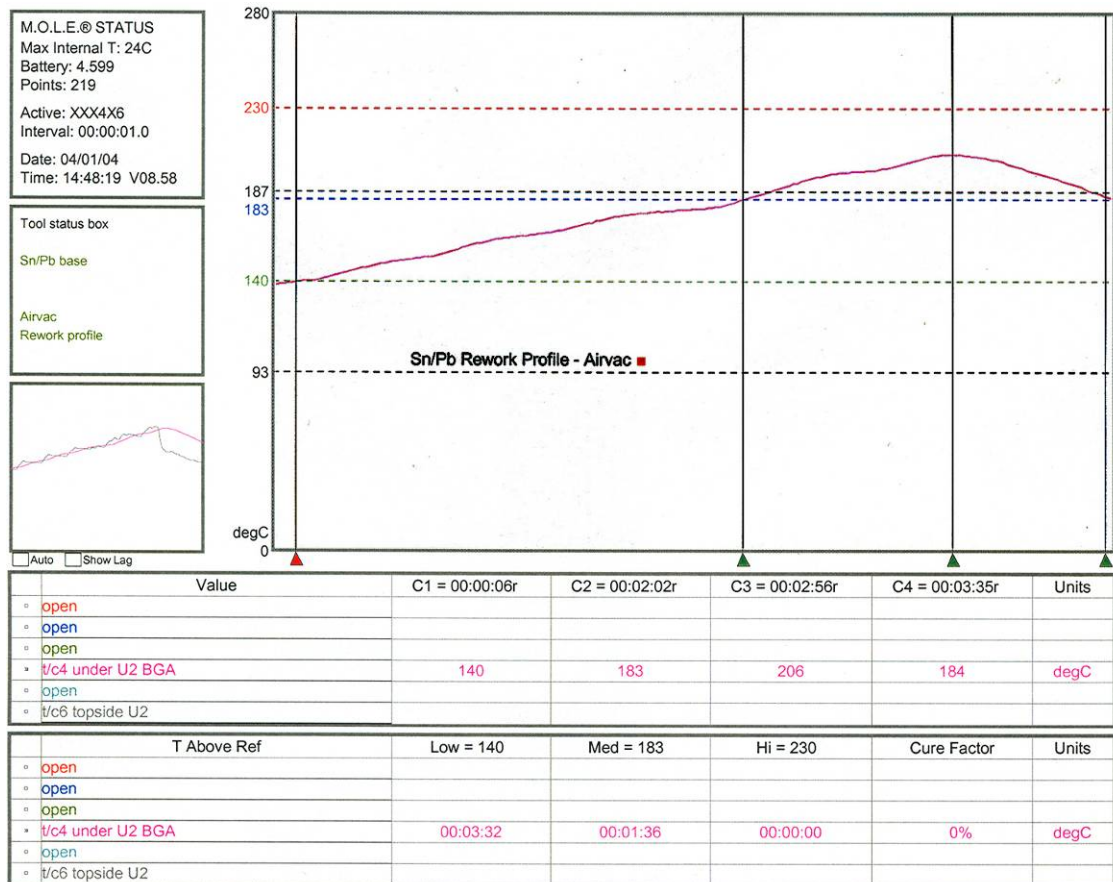


Figure 25 Example SnPb Rework Profile for area array components, removal and replacement

- **Lead-Free rework profile for area array removal and replacement**
 - Device joint target = 240°C +/- 5°C
 - Device top max target = 260°C
 - Board max = as measured by the board trigger thermal couple; will be recorded
 - Reflow:
 - ~60 - 120 seconds @ 170-205°C
 - ~60 - 120 seconds above liquidus of alloy
 - Delta T from center to corner ball = 10°C
 - Ramp rate = <4°C/sec

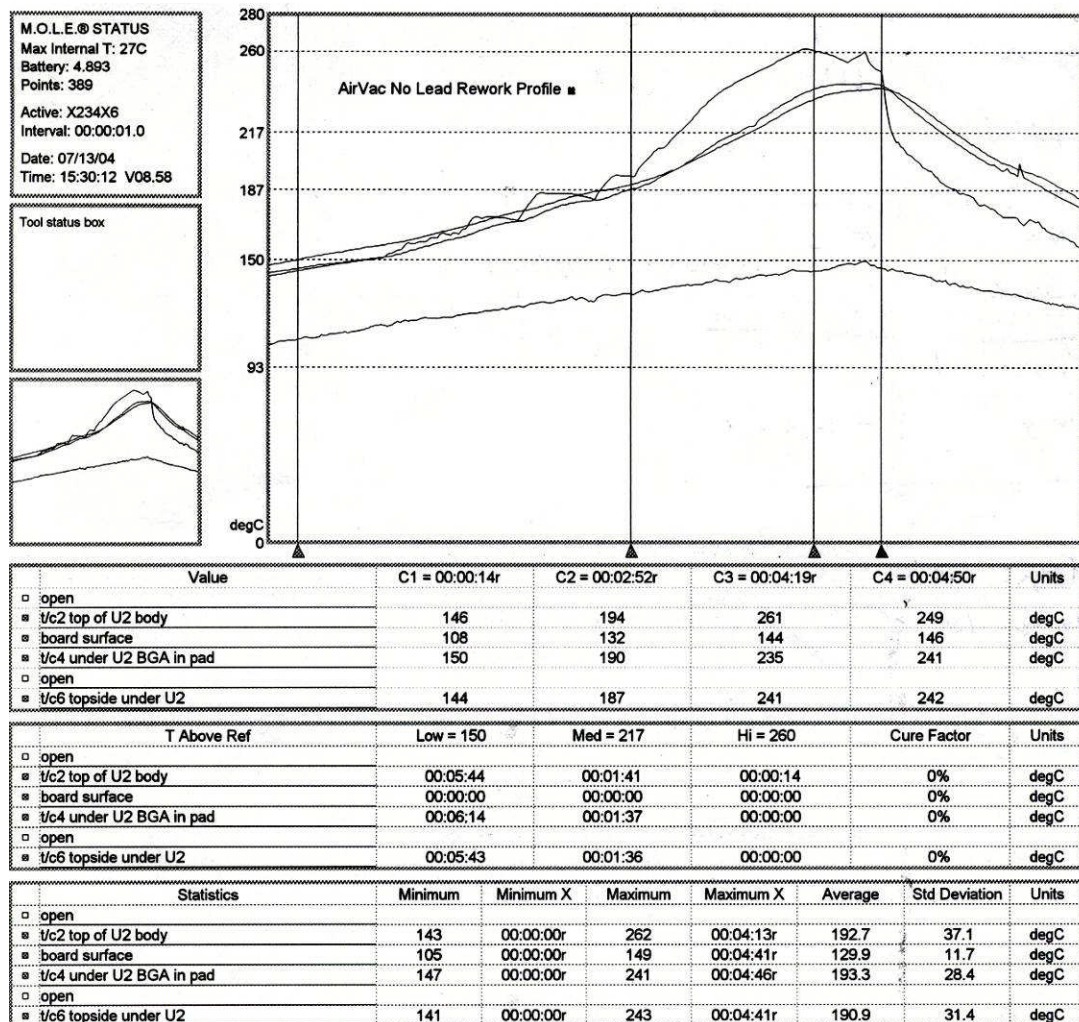


Figure 26 Example Lead-Free Rework Profile for area array components, removal and replacement

12.0 Thermal Aging, 100°C for 24 hours

The project consortia members reviewed intermetallic calculations generated by Rockwell Collins and compared the calculations to data sets from the Center for Advanced Vehicle Electronics (CAVE) at Auburn University, the National Physics Laboratory (NPL), the National Institute of Standards and Technology (NIST), and the Center for Advanced Life Cycle Engineering (CALCE) at University of Maryland. The thermal aging procedure was selected to establish a common, standard starting point such that all test vehicles were relatively equal in terms of solder joint microstructure, printed wiring board stress state, surface finish oxidation condition, and intermetallic phase formation/thickness. The project consortia members desired to have the test vehicles begin the various testing procedures with a common starting state point in an effort to eliminate potential assembly differences which could possibly inadvertently/unintentionally influence the testing results. The thermal aging procedure is not necessarily, nor intended to be, representative of the various burn-in, bake-out, or other environmental stress screening (ESS) procedures that are used to evaluate electronics hardware quality/functionality. Additionally, it should be noted that the thermal aging procedure being used by the NASA-DoD LFE Project consortia is not meant to be representative of operational field life. A wide range of ESS procedures and operational field expectations exist in the high performance electronics industry, from telecom applications to space applications, thus an industry consensus "standard" thermal aging procedure that fits all electronics users is not available.

13.0 Rework Test Vehicle Characterization

Following assembly and rework procedures, Rockwell Collins will cross-section the rework test vehicles set aside for characterization. One component from each of the 4 component types (BGA, CSP, PDIP, TSOP) being reworked from each of the 3 types of rework boards (SnPb, SnPb-ENIG, lead-free) will be cross sectioned.

Table 30 Rework Test Vehicles for Characterization

Project Activity	Batch / Board Number
Test Vehicle Characterization	Batch A / SN163
	Batch B / SN123
	Batch B / SN154

14.0 Testing Activities

The first step in developing the test plan was to review the performance requirements called out in applicable military and industry standards, and then select test methods recognized and agreed upon by the technical team members. A key factor was selecting test parameters that would subject enough environmental stress to cause solder joints to fail, thus permitting differentiation between lead vs. lead-free performance. Military document MIL-STD-810F and industry documents IPC-SM-785 and IPC-TM-650 were primary references used for writing the test plan. One test—the Combined Environments test—followed a procedure developed and used by Raytheon.

14.1 Vibration

The vibration test determines solder joint failures during exposure to vibration conditions. The stakeholders agreed that MIL-STD-810F, Method 514.5 (Vibration), would be the starting point for developing a vibration test that would determine the reliability of the various solder alloys under severe vibration. Specific details on the vibration test can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.2 Thermal Cycling

The thermal cycle testing determines the capability of a solder to withstand extreme thermal cycling. This test will be performed in accordance with IPC-SM-785 (*Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*).

Thermal cycling will be conducted at two different conditions, -55 to +125°C and -20 to +80°C, technical representatives from the U.S. Army Aviation and Missile Command (AMCOM) suggested two temperature ranges to allow for acceleration factors to be determined, which will permit extrapolation of the data to actual use conditions of their systems. The thermal cycle tests will be run until a significant number (greater than 63 percent) of component failures are achieved in order to provide statistically meaningful data. Specific details on the thermal cycle test can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.3 Mechanical Shock

The purpose of the mechanical shock test is to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by rough handling, transportation, or field operation. The mechanical shock test procedure was changed from the procedure used for the JCAA/JGPP Lead-Free Solder Project. The consortia members felt that the procedure change was necessary since it is very difficult to meet both the SRS shape and the pulse duration for this test as outlined in MIL-STD-810F. Pulse duration is approximately equal to the inverse of lowest SRS frequency, 10 Hz. SRS requirement means pulse duration >100 msec while MIL-STD-810F outlines pulse durations ≤ 23 msec. Additional details on the procedure change are contained in Appendix E. Specific details on the mechanical shock test can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.4 Combined Environments Test

The Combined Environments Test (CET) determines the reliability of solders under combined thermal cycle and vibration. The CET for the lead-free solder project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process. The project stakeholders felt that the CET would provide a quick method to identify comparative potential reliability differences in the test alloys vs. the SnPb baseline. The primary accelerated environments are temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom used in combination). Specific details on the combined environments test can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.5 Drop Testing

This test determines the resistance of board level interconnects to board strain induced by dynamic bending as a result of drop testing. Boards tested using this method typically fail either as interfacial fractures in the solder joint (most common with ENIG) or as pad cratering in the component substrate and/or board laminate. These failure modes commonly occur during manufacturing, electrical testing (especially in-circuit test), card handling and field installation. The root cause of these types of failures is typically a combination of excessive applied strain due to process issues and/or weak interconnects due to process issues and/or the quality of incoming components and/or boards. Specific details on the drop test can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.6 Interconnect Stress Test (IST)

IST is an industry recognized test method (IPC) that accelerates thermal cycling testing by heating a specifically designed test coupon to 150°C in exactly 3 minutes followed by cooling to ambient in approximately two minutes. IST test coupons have two circuits, a sense circuit and a power circuit, to monitor material delamination and crazing. The power circuit heats the coupon. The sense circuit is a passive circuit that monitors temperature and measures damage accumulation of the interconnect structure, typically a plated through-hole (PTH). There are usually 400 to 800 structures per circuit to achieve a higher, statistically relevant, sample size. Both the power and sense circuits changes in resistance (milliohms) and temperature (°C) throughout the coupons during the thermal cycle. Thermal cycling continues until end of test or a 10% increase in resistance on either circuit. Each coupon is heated, monitored, and tested individually. This gives a number of advantages that include no hold time at temperature, tight test control in the ability to achieve any test temperature in three minutes +/- 5 seconds, the ability to stop testing within seconds of the circuit achieving a 10% increase in resistance allowing analysis of a developing failure rather than a catastrophic failure. Testing stops immediately when the circuit achieves 10% increase in resistance, allowing a failed circuit to have a low amount of power applied that creates a hot spot at the failure site visible by a thermal imaging camera. Specific details on IST can be found in the JTP, “*NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007*”.

14.7 Copper Dissolution

The purpose of the copper dissolution testing is to characterize, document, and compare the impact of soldering process on the copper plated through-hole and surface pad structures for the NASA-DoD test vehicles with the SAC305 and SN100C solder alloy systems. The copper dissolution test results will provide a data set which can be used as a first order approximation of the copper plating thickness loss due to lead-free solder processing. Additionally, the copper dissolution test results can be compared to other published industry results for alternative solder alloy systems and different soldering processes.

Printed Circuit Board (PCB) land and plated through-holes can be eroded or dissolved away in the presence of molten solder rendering the PCB non-functional. Significant dissolution can occur with the use of certain new Sn-rich alloys and is further exacerbated

by higher process temperatures. Clearly this phenomenon represents a serious risk to circuit reliability. There is a clear need to determine the dissolution rate of copper pads with lead-free solders under various conditions. Specific details on copper dissolution can be found in the JTP, “NASA-DoD Lead-Free Electronics Project, Joint Test Protocol, October 8, 2007”.

15.0 Failure Analysis

The purpose of the failure analysis is to identify the failure mode and the most probable failure mechanism of the solder joints. Accordingly, solder alloy material integrity, composition, microstructure and metallurgical features specific to the type of alloy shall be investigated on all types of boards, hence all types of solders and termination finishes.

Failure analysis will be performed per the procedure outlined in 15.1 and will encompass visual, x-ray, micro-structural evaluation, and composition on a selected sampling of failed joints of components identified and recorded during stress testing.

In order to assure that metallurgical characteristics are relevant to the failure, reference samples of joints not detected as failed will also be evaluated. The reference samples (joints) will be selected from the same component. PCB pad condition and overall board material integrity condition at the failed component shall be evaluated as well.

15.1 Procedure

Failure analysis will not be done until all testing to any given environment is completed. Components will not be removed from the test vehicles during testing.

15.1.1 Sample Identification

Failure analysis procedure shall be performed per Figure 27. Components are identified by the following set of symbols:

1. PCB Number
2. Component type and reference designator for the assigned location on PCB.
Example: U18
3. Table number
Example: “Table 7”; the table number is the table of this document that lists component finish and solder type applied for attachment or rework. All components and solders for attachment and rework are listed in tables:
Table 7 Component Finish Matrix – Lead-Free Rework Test Vehicles (Batch A)
Table 9 Component Finish Matrix – SnPb Rework Test Vehicles (Batch B)
Table 11 Component Finish Matrix – SnPb Manufactured Test Vehicles (Batch C)
Table 13 Component Finish Matrix – SnPb Manufactured Test Vehicles (Batch D)
Table 15 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch E)
Table 17 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch F)

Table 19 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch G)

Table 21 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch H)

Table 23 Component Finish Matrix – Lead-Free Manufactured Test Vehicles (Batch I)

4. Identification number of failed solder joint/termination number as identified from the data sheet of the part, or UK (unknown) if the failed part termination or solder joint cannot be identified prior to cross-sectioning.
5. Acronym defining type of test the board was exposed to such as:
 - TC (thermal cycling)
 - CE (combined environmental)
 - V (vibration)
 - MS (mechanical shock)
 - DT (drop test)

The component solder joint location, material composition and testing history will be defined by the following set of symbols:

- **Example One: 1-BGA-U18-07-1-TC**

It translates into PCB Number 1, component BGA at the location U18, Table 7, failed pin solder joint number 1 and, post thermal cycling. In addition Table 7 specifies SAC405 as component finish and SAC305 reflow solder.

- **Example Two: 1-BGA-U18-07-UK-TC**

It translates into PCB Number 1, component BGA at the location U18, Table 7, failed pin solder joint not identifiable and, post thermal cycling. In addition Table 7 specifies SAC405 as component finish and SAC305 reflow solder.

15.1.2 Sample Size

The minimum number of components for failure analysis will be determined by the project stakeholders on test by test basis.

In the case where no components are identified as failed, a destructive physical analysis (DPA) will be performed. Procedures for DPA will be identical to the FA procedure specified in Figure 27. Statistical analysis of the test vehicle failure data for each test shall be used to identify potential candidate components for FA and DPA analysis. A minimum of 3 failed and 3 non-failed samples shall be analyzed from each of seven component types (BGA-225, CLCC-20, CSP-100, PDIP-20, QFN, TQFP-144, TSOP-50), from the SnPb and lead-free Manufactured test vehicles as well as the SnPb and lead-free Reworked test vehicles. For each component type (BGA-225, CLCC-20, CSP-100, PDIP-20, QFN, TQFP-144, TSOP-50), one of the 3 (minimum number) failed samples should be the last component to fail. All “outlier” test vehicle component failures, as determined by the statistical analysis, shall be analyzed. Additional samples (failed or non-failed) may be from the test vehicles and those results shall be included in the FA/DPA report.

Table 31 Example Failure Analysis Tracking Table (Batch C)

SnPb Manufactured: SN										
Component	Component Finish	Reflow Solder	Wave Solder	Board Finish	Sample Identification					
					Failed			Non-Failed		
BGA-225	SAC405	SnPb		Immersion Ag						
BGA-225	SnPb	SnPb								
CLCC-20	SAC305	SnPb								
CLCC-20	SnPb	SnPb								
CSP-100	SAC105	SnPb								
CSP-100	SnPb	SnPb								
PDIP-20	NiPdAu		SnPb							
PDIP-20	Sn		SnPb							
QFN	Matte Sn	SnPb								
TQFP-144	Matte Sn	SnPb								
TQFP-144	SnPb Dip	SnPb								
TSOP-50	SnBi	SnPb								
TSOP-50	SnPb	SnPb								

Table 32 Example Failure Analysis Tracking Table (Batch B)

SnPb Rework: SN _____												
Component	Component Finish	Reflow Solder	Wave Solder	New Component Finish	Rework Solder	Board Finish	Sample Identification					
							Failed			Non-Failed		
BGA-225	SAC405	SnPb		--	--	Immersion Ag						
BGA-225	SnPb	SnPb		SAC405	SnPb							
BGA-225	SnPb	SnPb		SnPb	Flux Only							
CLCC-20	SAC305	SnPb		--	--							
CSP-100	SAC105	SnPb		--	--							
CSP-100	SnPb	SnPb		SAC105	SnPb							
CSP-100	SnPb	SnPb		SnPb	Flux Only							
PDIP-20	NiPdAu		SnPb	--	--							
PDIP-20	Sn		SnPb	--	--							
PDIP-20	SnPb		SnPb	Sn	SnPb							
QFN	Matte Sn	SnPb		--	--							
TQFP-144	NiPdAu	SnPb		--	--							
TQFP-144	SnPb Dip	SnPb		--	--							
TSOP-50	SnBi	SnPb		--	--							
TSOP-50	SnPb	SnPb		--	--							
TSOP-50	SnPb	SnPb		SnPb	SnPb							
TSOP-50	SnPb	SnPb		Sn	SnPb							

15.1.3 FA/DPA Component Preparation

Components on intact test vehicles

1. Component identification/labeling with labels as specified in 15.1.1
2. Visual evaluation of the component body and solder joints material integrity.
3. An overall photo of the test vehicle capturing component location / orientation is required
4. Photographing typical appearance of the failed and non failed solder joints
 - a. Photographs of disturbed component trends
 - b. Magnifications should be recorded by the FA / DPA facility
 - c. The analyst has the freedom to chose the proper micrograph to reveal the anomaly or region of interest found at a particular magnification
5. X-Ray evaluation of the test vehicles and failed/non-failed solder joints shall be conducted. The X-Ray equipment and technique shall be identified in the FA/DPA report.
 - a. The analyst has the freedom to choose the proper micrograph to reveal the anomaly or region of interest.
6. Thermal imaging for identification of failed solder joints not identifiable by visual or x-ray techniques may also be conducted if the necessarily resources are available. The thermal imaging equipment and technique shall be identified in the FA/DPA report.
7. For array components (BGA and CSP) characterize corner and die-shadow joints. This can be done by metallographic cross-section or dye and pry.

Following the evaluation of the components they will be removed from the test vehicles in accordance with ASTM E3.

1. Suggested metallographic analysis procedure:
 - a. Each component with failed solder joint shall be positioned into a mould in orientation perpendicular to the grinding plane and potted in a two part 24 [h] epoxy (Buehler Epo-resin and Epo-hardener). Grinding will be performed by the following technique: 180 grit, 240 grit, 400 grit, 800 grit, and 1200 grit. Polishing by 6 [μ] diamond and 0.05 [μ] alumina.
 - b. Colloidal silica is highly recommended for final polishing

15.1.4 Analysis

FA and DPA procedures shall be performed per Figure 27. The statistical analysis of the test vehicles shall be provided by the testing organization/facility to the FA/DPA facility. Additional failed and non-failed components above the stated minimums may be done by the cognizant FA/DPA facility.

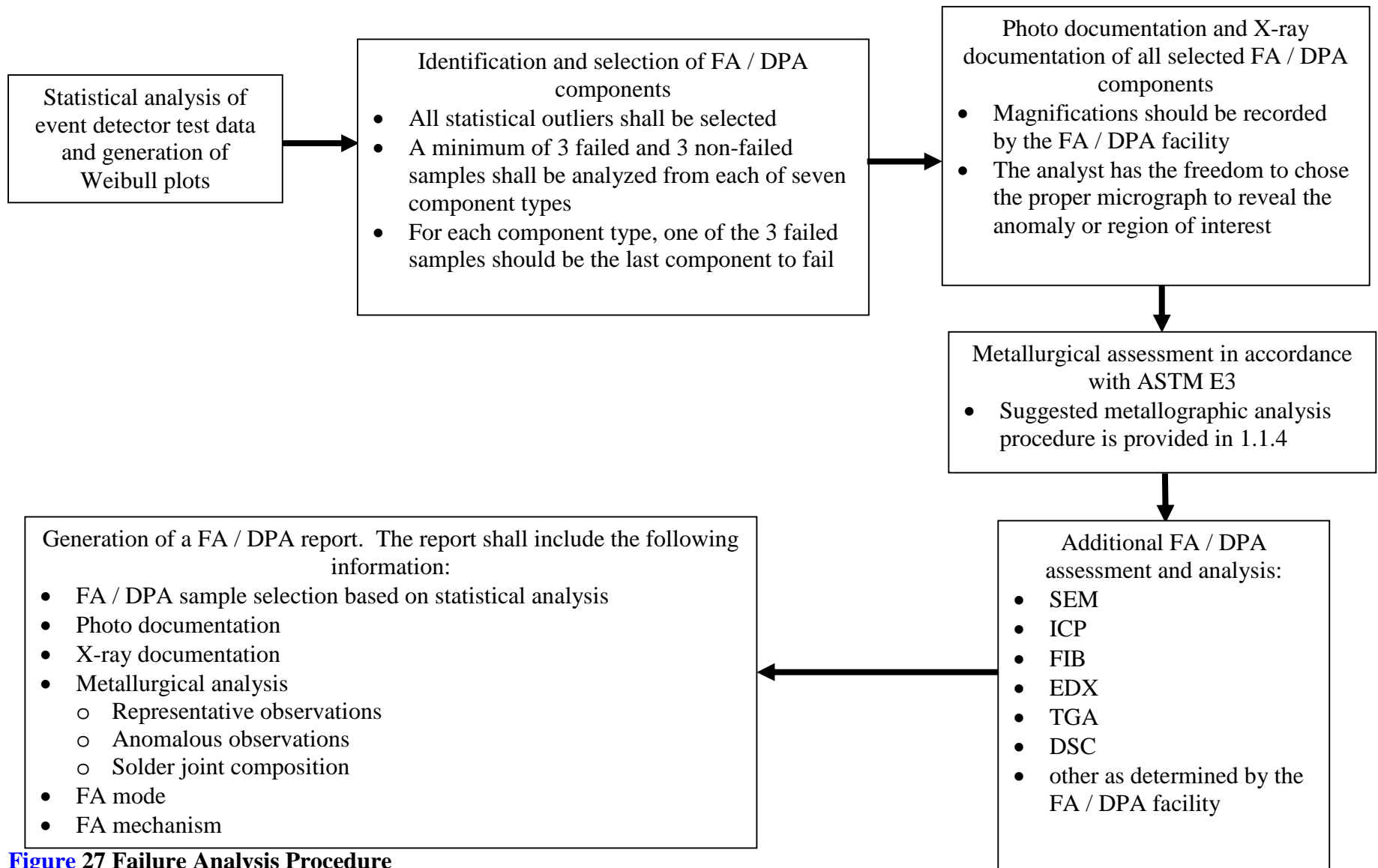


Figure 27 Failure Analysis Procedure

16.0 References

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 2. D. Hillman, M. Wells, K. Cho, "The Impact of Reflowing A Pbfree Solder Alloy Using A Tin/Lead Solder Alloy Reflow Profile On Solder Joint Integrity", Lead-Free Conference, CMAP Toronto, May 2005.
- IPC 6012B: Qualification and Performance Specification of Printed Circuit Boards August 2004
 - IPC 45101B: Specification for Base Materials for Rigid and Multilayer Printed Boards
 - MIL-STD-810F: Environmental Engineering Considerations and Laboratory Tests January 2000
 - IPC/EIA J-STD-001C: Requirements for Soldered Electrical and Electronic Assemblies March 2000
 - IPC SM 785: Guidance for Accelerated Reliability Testing of Surface Mount Solder Attachments Nov. 1992
 - IPC-9701: Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments February 2006
 - IPC TM 650:
 - NASA STD 8739.2: Workmanship Standard for Surface Mount Technology
 - IPC 9252: Guidelines and Requirements for Electrical Testing of Unpopulated Boards, Jan 2001
 - ANSI/J-STD-003: Solderability Test for Printed Boards
 - IPC-2221: Generic Standard on Printed Board Design
 - IPC-2222: Sectional Design Standard for Rigid Organic Printed Boards
 - IPC-A-610D: Acceptability of Electronic Assemblies
 - IPC-4101B: Specification for Base Materials for Rigid and Multilayer Printed Boards
 - IPC-7711: Rework of Electronics Assemblies

Appendix A - TSOP components without dummy die

One of the dominate failure modes of solder joints in the electronics industry is the loss of solder joint integrity due to coefficient of thermal expansion (CTE) mismatch. The typical printed wiring board is an epoxy laminate material with a CTE of 16 ppm/°C, the CTE of a component silicon die is 6 ppm/°C, the CTE of copper is 16 ppm/°C and the CTE of eutectic tin/lead solder that comprises a solder joint is 24 ppm/°C. Reviewing the differences in CTE values reveals that there is a local CTE mismatch between the printed wiring board and the component with the solder joint taking the brunt of the thermally induced dimensional changes. The impact of CTE mismatch on a solder joint can be demonstrated as a worst and best case scenario for two component types: Leadless Ceramic Chip Carriers (LCCC) and Quad Flat Packs (QFP). An LCCC is a ceramic bodied component with solder connections directly to the printed wiring board without the benefit of a compliant lead. An LCCC has a CTE of 6 ppm/°C and the epoxy laminate printed wiring board a CTE of 16 ppm/°C – a significant CTE mismatch which results in the severe degradation of solder joint integrity and is the worst case example. A QFP is a plastic bodied component with a compliant lead construction. A QFP has a CTE of 16 ppm/°C, the copper lead a 16 ppm/°C, the eutectic tin/lead solder a 24 ppm/°C and the epoxy laminate printed wiring board a CTE of 16 ppm/°C – a relatively matched CTE set of materials which does not result in severe degradation of solder joint integrity and is the best case example. The inclusion of dummy silicon die in many components is an important factor in replicating solder joint degradation due to CTE mismatch conditions.

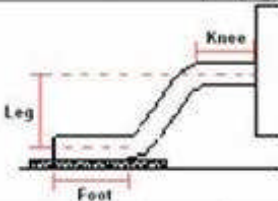
The NASA-DoD Lead-Free Electronics Project included a thin small outline package (TSOP) which utilized an iron/nickel leadframe material instead of the typical copper leadframe material. The TSOP component configuration was selected because the iron/nickel leadframe material, with a CTE of 6 ppm/°C, induced the same severe solder joint degradation as a ceramic bodied component but in a more widely industry utilized package type. The iron/nickel leadframe material CTE mismatch induced solder joint degradation is very useful in terms of DOE investigation failure benchmarking. The NASA-DoD Lead-Free Electronics Project consortia was confronted with a component procurement issue for the TSOP components due to daisy chain configuration problem. A source of TSOPs was found with an acceptable daisy chain configuration for testing. Unfortunately, the acceptable daisy chain TSOPs did not contain a dummy silicon die. However, the iron/nickel leadframe material induced CTE mismatch is the dominate CTE mismatch driving force in comparison to the dummy silicon die induced CTE mismatch for the TSOP component. Other industry investigations [1-3] have demonstrated this parameter influence for the TSOP component with iron/nickel leadframe. The NASA-DoD Lead-Free Electronics Project consortia proceeded with the procurement of the TSOP components without dummy die for the investigation based on this component assessment.

References:

1. J. Lau, S. Golwalkar, P. Boysan, R. Surratt, R. Forhringer, S. Erasmus, “Solder Joint Reliability of a Thin Small Outline Package (TSOP)”, Circuit World, Volume 20, Number 1, 1993.
2. W. Engelmaier and B. Fuentes, “Alloy 42- A Material to be Avoided for Surface Mount Component Leads and Lead Frames”, Soldering & Surface Mount Technology, Volume 21, October, 1995.
3. J. Lau and Y. Pao, Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, ISBN 0-07-036648-9, McGraw Hill, 1997, page 329-356.

Appendix B - Example Component Characteristic Worksheet

Package:

Feature	Value
Package length	metric mm (english inch)
Package width	metric (english)
Package thickness	metric (english)
Pitch	metric (english)
Mass	g
CTE (Moire method for BGA & CSP, otherwise TMA method)	ppm/°C
Die length	metric (english)
Die width	metric (english)
Die thickness	metric (english)
Lead width	metric (english)
Lead thickness	metric (english)
Minimum lead gap	metric (english)
	
Lead foot length	metric (english)
Lead leg length	metric (english)
Lead knee length	metric (english)

Feature	Value
Lead/Termination Base Metal Alloy	Alloy
Lead/Termination Metallization / thickness	Alloy/metric (english)
Plating 1 metallization / thickness	Alloy/metric (english)
Plating 2 metallization / thickness	Alloy/metric (english)
Plating 3 metallization / thickness	Alloy/metric (english)
Over-plate to protect during cross section?	yes/no, plating
Diameter of solder balls	metric (english)
Solder ball alloy (SEM or XRF estimate)	
Width of solder ball in contact w/ component pad	metric (english)
Width of component pad	metric (english)
Thickness of component pad	metric (english)
Diameter of solder mask opening	metric (english)
Daisy chain pattern has been confirmed (daisy chain even pattern 1-2, 3-4, etc.)	yes/no

Insert image here and resize if necessary
X-ray

Insert image here and resize if necessary
Top View

Insert image here and resize if necessary
End View/Bottom View

Insert image here and resize if necessary
Cross-section of (fill in mag here.X)

Insert image here and resize if necessary
SEM of cross-section

Appendix C - Test Vehicle Drawings

NOTES:

- THE SYMBOL T DESIGNATES PRINTED BOARD TOP SURFACE. CIRCUIT LAYERS ARE VIEWED AND NUMBERED FROM THE TOP SURFACE.
- MATERIAL:
 - LAMINATE AND PREPREG CONSTRUCTION: SEE DETAIL A.
 - LAMINATE AND PREPREG BASE MATERIAL SHALL BE IN ACCORDANCE WITH IPC-1107/2B (FR-4) WITH A TG OF 170 DEGREES C MINIMUM. PRINTED BOARD MAY BE FABRICATED FROM LAMINATE, PREPREG, OR ANY COMBINATION TO MEET THE REQUIREMENTS SPECIFIED HEREIN.
 - METAL FOIL SHALL BE COPPER TYPE C, D, OR H.
- FABRICATION, INSPECTION AND QUALITY REQUIREMENTS SHALL BE IN ACCORDANCE WITH IPC-6012, LATEST REVISION, CLASS 3, TYPE 3, AND THIS DRAWING.
 - POSITIVE ETCH-BACK OR SHEAR REMOVAL IS REQUIRED.
 - HOLDING, OR EDGE DELAMINATION, MAY EXTEND TO CONDUCTORS LOCATED WITHIN .100 OF BOARD EDGE.
 - CIRCUIT CONTINUITY TESTING IS REQUIRED.
- FINAL FINISH SHALL BE IMMERSION SILVER, .000008 - .000016 INCH (.2 - .4 MICROMETER THICK, USING MODERNOID INC., STERLING[VA] IMMERSION SILVER DEPOSITION PROCESS.
- ETCH, OR EQUIVALENT MARKING PROCESS, THE FOLLOWING INFORMATION IN THE APPROXIMATE LOCATION INDICATED ON THE PRINTED BOARD IN ACCORDANCE WITH MIL-STD-130. THE PREFERRED METHOD OF MARKING IS ETCHING. IF INK IS USED, IT SHALL BE OF A CONTRASTING COLOR, TYPE PAS6032-II IN ACCORDANCE WITH R-R-56032, OR EQUIVALENT. CHARACTER SIZE FOR THE FOLLOWING INFORMATION SHALL BE APPROXIMATELY .080 HIGH USING .012 LINE WIDTHS.
 - REVISION LETTER FOLLOWING THE LETTERS REV
 - MANUFACTURING DATE CODE FOLLOWING THE LETTERS MFR
 - CALENDARY YEAR AND PLATING WEEK LOT COMPLETION DATE.
 - VARIABILITY MARKINGS FROM THE PANEL TO THE PRINTED BOARD TO THE COUPONS.
- APPLY SOLDER MASK OVER BARE COPPER OR OVER IMMERSION SILVER TO THE TOP AND BOTTOM SURFACES OF THE PRINTED BOARD IN ACCORDANCE WITH ANSI/JPCA-SM-84D, CLASS H, WITH THE FOLLOWING ADDITIONS:
 - COLOR: GREEN
 - REGISTRATION: ALL CONDUCTORS WITHIN THE AREA DEFINED BY SOLDER MASK REGISTRATION SHALL BE COVERED INCLUDING CONDUCTORS ADJACENT TO PLATED THROUGH HOLES. MINIMUM SOLDER MASK CLEARANCE FOR PLATED THROUGH HOLES SHALL BE .002 TO THE EDGE OF HOLE; NO SOLDER MASK IS ALLOWED ON SURFACE MOUNT LAND AREAS.
- TOLERANCES: UNLESS OTHERWISE SPECIFIED, FINISHED PRINTED BOARD TOLERANCES:
 - LOCATION TOLERANCES:
 - NON-PLATED HOLES TO NON-PLATED HOLE OR PLATED HOLE TO PLATED HOLE
-.003, -.003
 - NON-PLATED HOLE TO PLATED HOLE
-.008, -.008
 - ANY HOLE TO NON-PLATED EDGE
-.008, -.008
 - NON-PLATED EDGE TO NON-PLATED EDGE
-.010, -.010
 - CHAMFERS AND CORNER RADIUS
-.008, -.008
 - FEATURE TOLERANCES:
 - PLATED HOLE DIAMETER
-.003, -.005
 - NON-PLATED HOLE DIAMETER
-.005, -.005
 - SLOT WIDTHS (.060 AND .093 WIDE)
 - CONDUCTOR WIDTHS:
 - < .008
.008 TO < .012
.012 TO .030
> .030
 - .001, -.001
.002, -.002
.002 TO .003
.002, -.004
- UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES.
- DRAWING LETTERS CODED A AND F ARE VISIBLE AND SHALL NOT BE PLATED SHUT.
- PARENT/CALL INFORMATION IS FOR REFERENCE ONLY.

SYMBOLS IN PARENTHESES NOT SHOWN IN SUBSEQUENT SHEETS

SYM	DRILL NAME	DRILLED DIA	FINISHED DIA	NOTES	PLATED	LAYERSET	QTY
B	P008	.0074 MIN	-----	9	YES	1-6	8014
F	F010	.0101 MIN	-----	9	YES	1-6	182
Z	P036	-----	.031-.036	-----	YES	1-6	340
A1	P243	-----	.238-.243	-----	YES	1-6	25
B6	N078	-----	.077-.081	-----	NO	1-6	3
BL	N091	-----	.089-.099	-----	NO	1-6	4
C9	N102	-----	.115-.128	-----	NO	1-6	4
D8	N150	-----	.151-.161	-----	NO	1-6	20

NON-PLATED HOLE LOCATIONS

	Coord	X	Coord	Y
B8	2.475	0.500		
B9	13.750	0.500		
B10	1.625	0.500		
B11	14.425	0.500		
B12	14.425	0.500		
B13	8.250	0.500		
B14	8.250	0.500		
B15	12.400	0.725		
B16	1.625	0.725		
B17	1.625	1.000		
B18	1.625	1.000		
B19	1.625	1.000		
B20	6.000	0.750		
B21	6.000	0.750		
B22	10.000	0.500		
B23	10.000	0.500		
B24	13.750	0.500		
B25	13.750	0.500		
B26	14.425	0.500		
B27	14.425	0.500		
B28	14.425	0.500		
B29	14.425	0.500		
B30	14.400	8.500		

DETAIL A

DETAIL B

DETAIL C

SEE NOTE 2

SEE DETAIL C

SEE DETAIL D

SEE DETAIL E

SEE DETAIL F

SEE DETAIL G

SEE DETAIL H

SEE DETAIL I

SEE DETAIL J

SEE DETAIL K

SEE DETAIL L

SEE DETAIL M

SEE DETAIL N

SEE DETAIL O

SEE DETAIL P

SEE DETAIL Q

SEE DETAIL R

SEE DETAIL S

SEE DETAIL T

SEE DETAIL U

SEE DETAIL V

SEE DETAIL W

SEE DETAIL X

SEE DETAIL Y

SEE DETAIL Z

SEE DETAIL AA

SEE DETAIL AB

SEE DETAIL AC

SEE DETAIL AD

SEE DETAIL AE

SEE DETAIL AF

SEE DETAIL AG

SEE DETAIL AH

SEE DETAIL AI

SEE DETAIL AJ

SEE DETAIL AK

SEE DETAIL AL

SEE DETAIL AM

SEE DETAIL AN

SEE DETAIL AO

SEE DETAIL AP

SEE DETAIL AQ

SEE DETAIL AR

SEE DETAIL AS

SEE DETAIL AT

SEE DETAIL AU

SEE DETAIL AV

SEE DETAIL AW

SEE DETAIL AX

SEE DETAIL AY

SEE DETAIL AZ

SEE DETAIL BA

SEE DETAIL BB

SEE DETAIL BC

SEE DETAIL BD

SEE DETAIL BE

SEE DETAIL BF

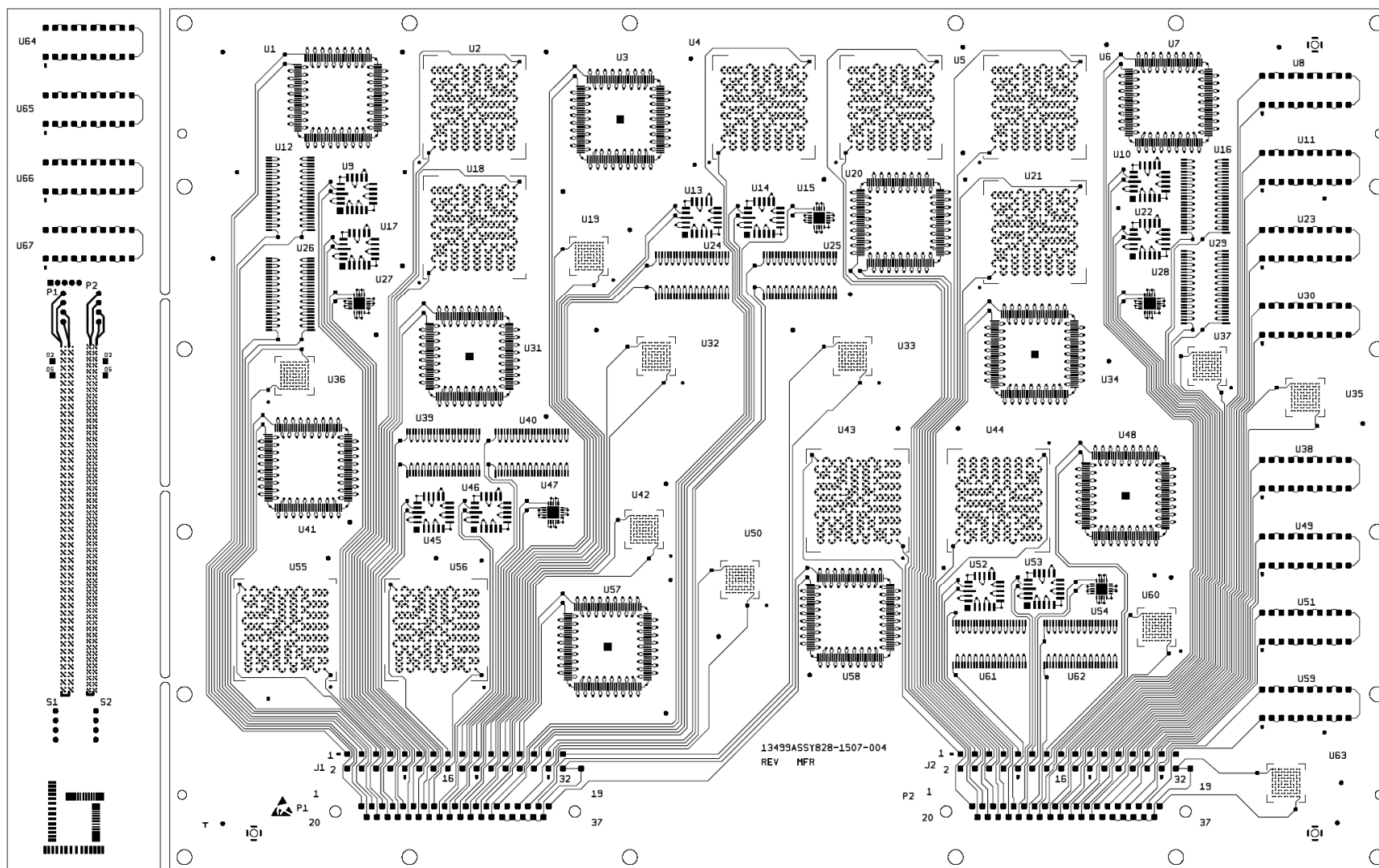
SEE DETAIL BG

SEE DETAIL BH

SEE DETAIL BI

SEE DETAIL BJ

SEE DETAIL BK</



Appendix D - NAVSEA Crane Assembly and Rework Effort

Crane Division, Naval Surface Warfare Center, a NASA-DOD Consortium member, is adding 30 test vehicles to the NASA-DOD study in support of their Naval Supply Command (NAVSUP) sponsored “Logistics Impact of Lead-Free Circuits/Components” project.

The NAVSEA Crane project through collaborative efforts with Science Applications International Corporation, Purdue University, and New Mexico Institute of Technology is analyzing data and building a database of publicly available reliability results from consumer, military, and aerospace electronics in order to assist the industry in quantifying the risks associated with choices of materials, processes, components and assemblies for Pb-free and mixed solder applications. This collaborative research and development project in lead-free soldering has specific relevance to the reliability of rework and repair processes of new Pb-free, legacy SnPb, and mixed solder systems using various combinations of Pb-free and legacy finished components and solder alloys in military systems.

The goal of the Crane NAVSUP project is to:

- develop a critical evaluation of new/existing reliability data as it is developed,
- to fill research gaps in tin whisker formation,
- examine rework of Pb-free and Sn-Pb solder joints, looking for microstructure evidence of damage in reworked solder joints,
- and to assist in developing a strategy for DoD on military electronics affected by the lead free initiative

The primary purpose of the 30 test vehicles add-on is to perform multiple pass SnPb rework 1 and 2 times on random Pb-free DIP, TQFP-144, TSOP-50, LCC and QFN components from SAC305 and SN100C soldered assemblies.

In a related test, the Crane project plans to stiffen the 9 Salt Fog test vehicles from the JCAA/JGPP Lead-Free Solder Project to military specifications and rerun the vibration test previously performed. The Crane project would like to see how standard circuit board stiffening affects the vibration test results previously observed.

NOTE: The Salt Fog board residues remained on the boards for over two years, etching the solder joints on the 9 test vehicles to varying degrees. The QFP-208 solder joints look very poor. Others look acceptable. The Crane project is aware of this issue and will take this into account when comparing data to un-stiffened boards.

The breakdown of the 30 test vehicles is as follows:

24 each built with SAC305
06 each built with SN100C

The reworked test vehicles will be integrated into the NASA-DOD -55°C to +125°C thermal cycling (Rockwell Collins), vibration (New Mexico Tech) and drop testing (Celestica) wherever space permits, to minimize variation between the NASA-DOD and Crane test data. Where NASA-DOD testing facilities cannot accommodate the Crane test vehicles, testing will be performed by New Mexico Institute of Technology using facilities at White Sands Missile Test Range.

The breakdown of the test vehicles is as follows:

Thermal Cycling -55°C to +125°C

- 4 each SAC305
- 4 each SN100C)

Vibration Testing (9 each SAC305)

Drop Testing (9 each SAC305)

Reserved for as manufactured testing, control and rework process development

- 2 each SAC305
- 2 each SN100C

The goal of this testing is to generate initial data supporting the qualification of existing SnPb rework procedures for all military hardware built with Pb-free processes through analysis of thermal cycling, vibration, and drop test data, with subsequent microsection analysis. Questions to be answered by this testing include:

1. Effect of X1, X2 and X3 rework on assembly reliability as tested by thermal cycle, vibration, and drop test.
2. Are Pb-free assemblies reworked with SnPb as reliable as as-built lead free hardware?
3. How residual Pb-free solder contamination levels in SnPb joints after X1, X2 and X3 rework correlate to reliability? (each rework cycle should reduce contamination levels) and analysis of solder samples will tell residual levels)
4. Effect of X1, X2 and X3 SnPb rework on surface mount land thickness (copper erosion) by cross section.
5. Visual evidence of X1, X2 and X3 rework damage to 170T_g laminate.

Test Vehicle Break Out

Due to the various types of test vehicles being assembled, BAE Systems will assemble the test vehicles in multiple batches.

Table 5 Test Vehicle Batch Key

[Batch F](#);

[Batch I](#)

Appendix E - Mechanical Shock Procedure Change

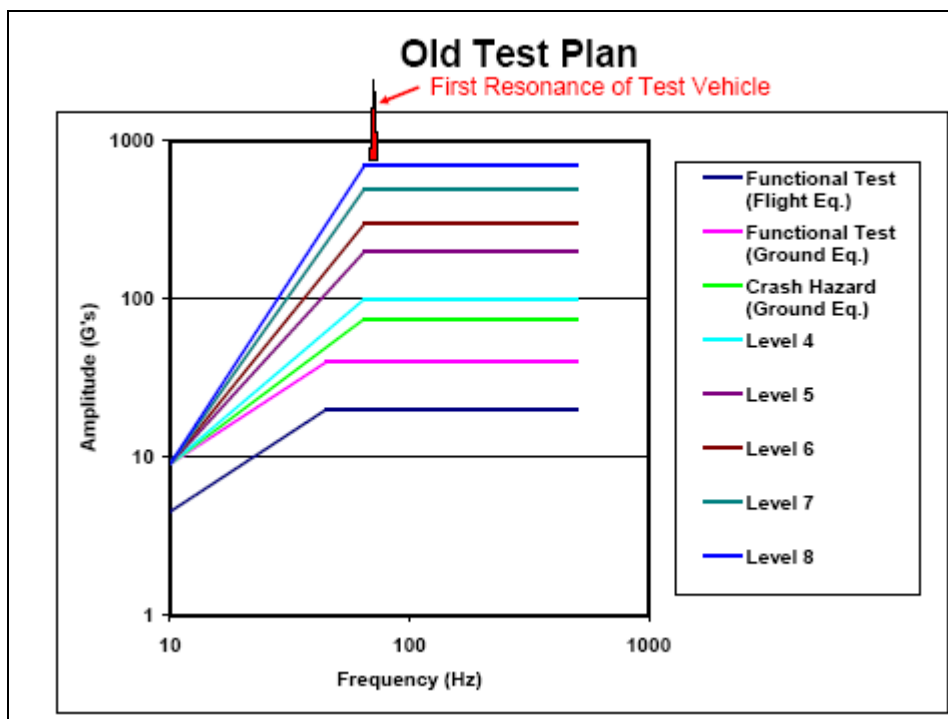
 **Engineering, Operations & Technology**
Phantom Works



Mechanical Shock Test Plan

Tom Woodrow
Boeing Phantom Works
Seattle, WA

NASA/DoD Lead-Free Electronics
Project Meeting
June 7, 2007

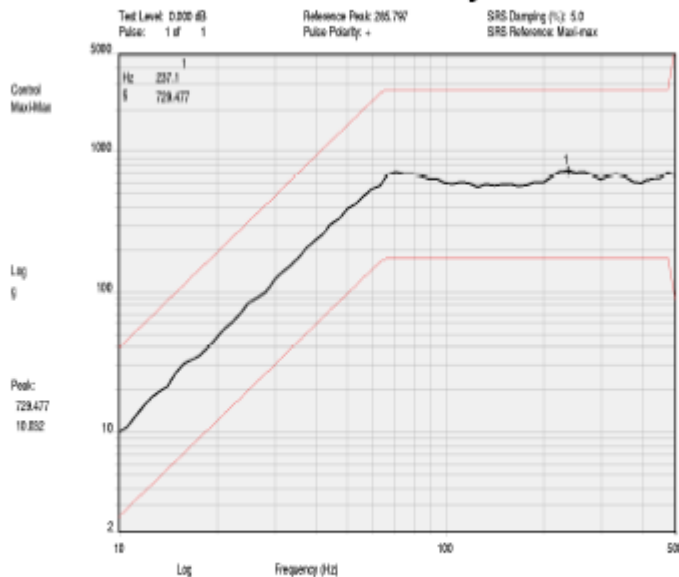
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Old Test Plan

Test	Initial G	Slope	Peak G	Ts (ms)	Cross-Over Freq.*	Shocks
Functional Test for Flight Eq.	4.5	6.0	20	15-23	45	100
Functional Test for Ground Eq.	9.0	6.0	40	15-23	45	100
Crash Hazard Test for Ground Eq.	9.0	6.8	75	8-13	65	100
Level 4	9.0	7.75	100	15-23	65	100
Level 5	9.0	9.97	200	15-23	65	100
Level 6	9.0	11.28	300	15-23	65	100
Level 7	9.0	12.92	500	15-23	65	100
Level 8	9.0	14.00	700	15-23	65	100 or more till majority fail
* Cross-over freq. may change dependent on resonant frequency of TV						

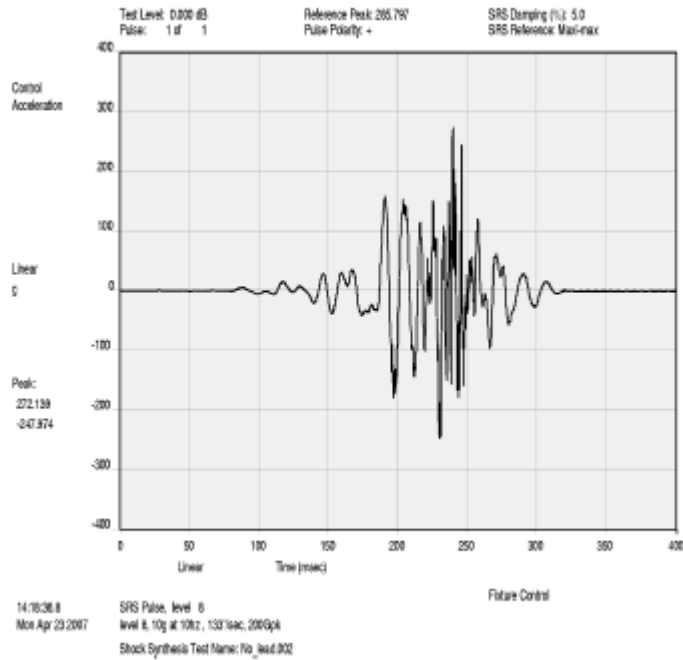
It is very difficult to meet both the SRS shape and the pulse duration for this test (even with explosives). Pulse duration approximately equals inverse of lowest SRS frequency. 10 Hz SRS requirement means pulse duration >100 msec.

Old Test Plan – Level 8 – Electrodynamics Shaker SRS

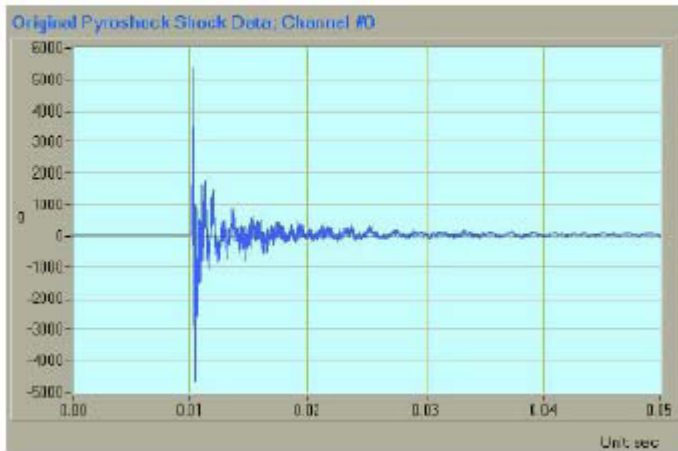


14-18-26.8
Mon Apr 23 2007
SRS Pulse, level 8
level 8, 10g at 10Hz, 130'/sec, 200Gpk
Shock Synthesis Test Name: No_Jed.802

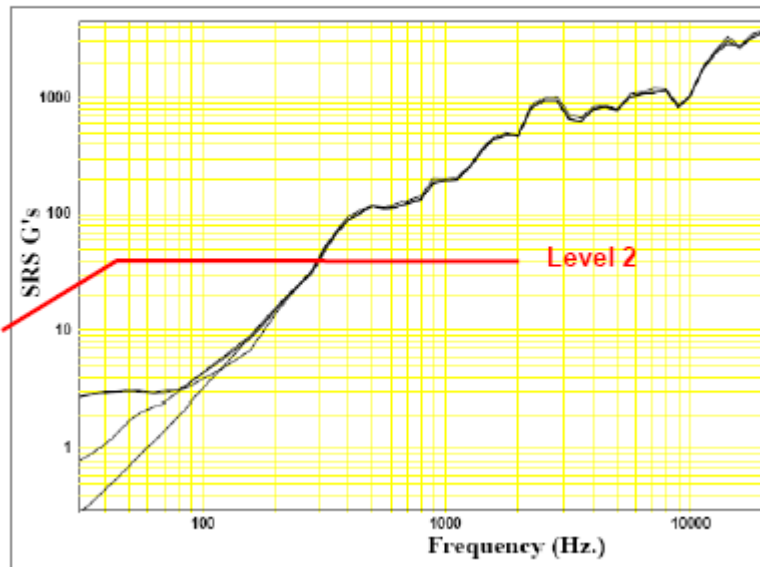
Old Test Plan – Level 8 – Pulse duration is too long



Pyrotechnic Shock Pulse Example – Duration Meets MIL-STD-810F



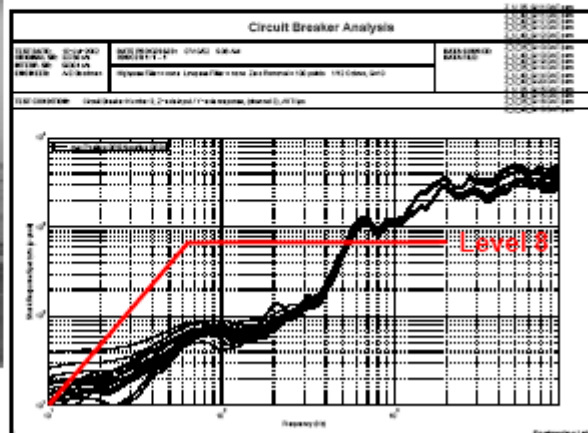
Pyrotechnic Shock SRS – does not satisfy MIL-STD-810F – very hard to control SRS shape – very expensive



Pendulum Shock Test Machine Boeing Structural Dynamics Lab



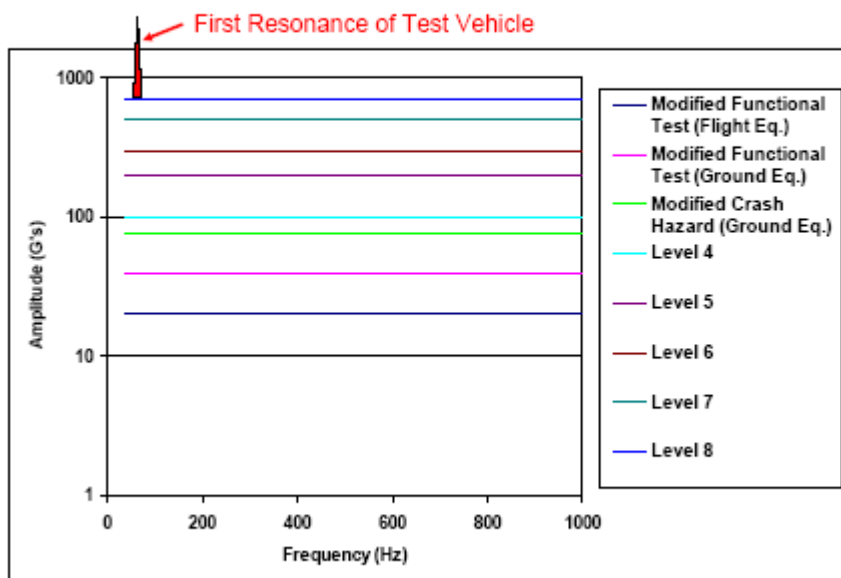
Designed to simulate pyrotechnic shock – notice that intermediate frequencies are missing – very hard to control SRS shape



MIL-STD-810F

“If the test item has no significant low frequency modal response, it is permissible to allow the low frequency portion of the SRS to fall out of tolerance in order to satisfy the high frequency portion of the SRS, provided the high frequency portion begins at least one octave below the first natural mode frequency of the test item.”

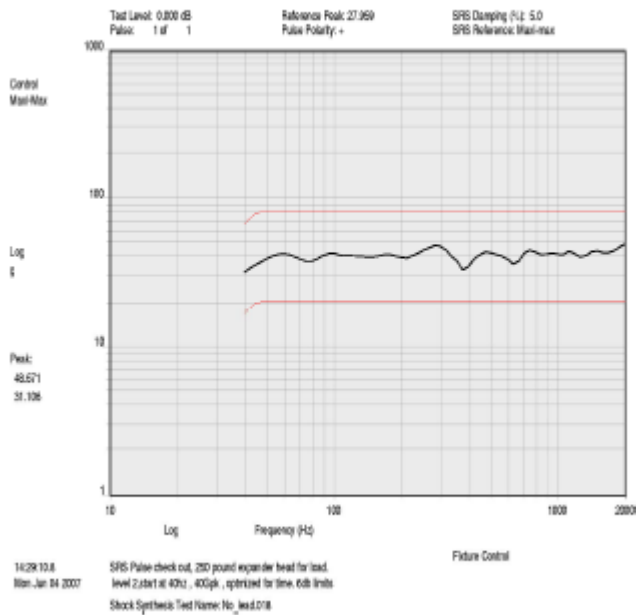
Modified Test Plan - SRS Inputs



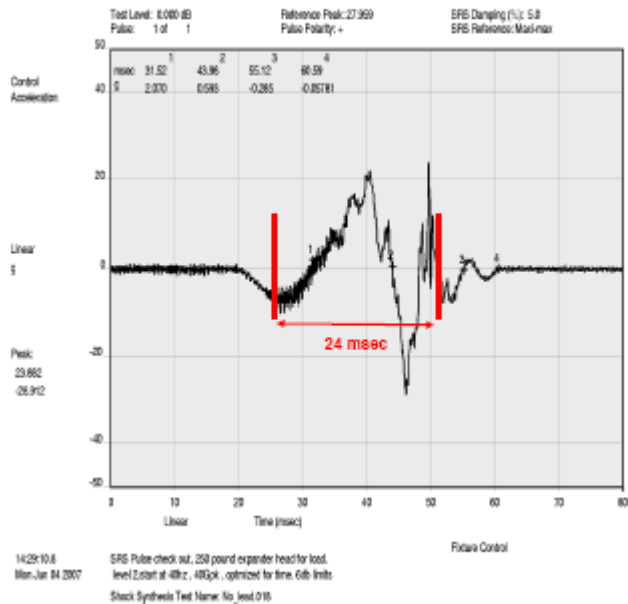
Modified Test Plan

Test	Amplitude (G's)	T _e (milliseconds)	Shocks Per Level
Modified Functional Test for Flight Eq.	20	<30	100
Modified Functional Test for Ground Eq.	40	<30	100
Modified Crash Hazard Test for Ground Eq.	75	<30	100
		<30	
Level 4	100	<30	100
Level 5	200	<30	100
Level 6	300	<30	100
Level 7	500	<30	100
Level 8	700	<30	100 or more till majority fail
* Cross-over freq. may change dependent on resonant frequency of test vehicle			

Modified Test Plan – Level 2



Modified Test Plan – Level 2



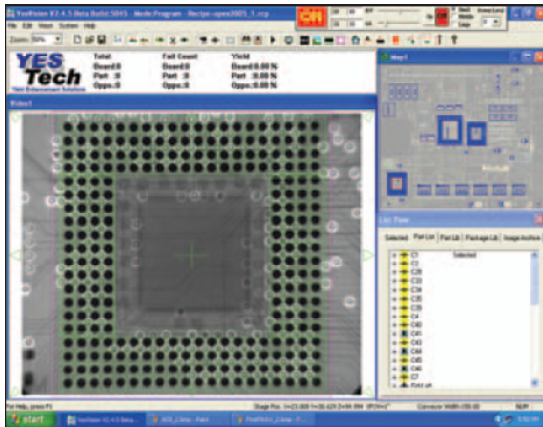
- Modified test plan ensures:
 - All major bending modes will be excited (not true for pyroshock or pendulum shock)
 - Good control of the SRS shape is maintained (not true for pyroshock or pendulum shock)
 - Pulse duration and SRS shape called out in MIL-STD-810F will be closely approximated

Appendix F- Area Array X-Ray Analysis Parameters

Machine:

YESTech YTX-5000 model in-line x-ray machine

- X-Ray Tube:
 - Sealed reflection target
 - 130 Kv, 5 micron spot size
 - 39-watt max. output
- X-Ray FOV:
 - 0.2” to 1.5” variable



Program settings:

All x-ray inspections are performed at 75kV and 40 μ A.

- Inspection set-up:
 - QFN
 1. Inspect each lead bank for joint presence and bridging
 - Threshold = 172
 2. Inspect center pad for voids (flag if > 25%)
 - Threshold = 151
 - CSP-100
 1. Inspect blocks of balls (5 x 5) for presence and bridging
 - Threshold = 120
 2. Inspect shape of individual balls for consistency
 - Threshold = 120
 - Shape Limit = 1.45
 3. Inspect size of individual balls
 - Threshold = 120
 - Size Range = .125 mm² - .175 mm²
 - Translates to \varnothing range of approx. 0.40 mm – 0.47 mm
 - Loose component ball size is 0.46 mm
 - Average x-ray ball size is .45 mm
 4. Inspect individual balls for voiding (flag if > 10%)
 - Threshold = 100
 - BGA-225
 1. Inspect blocks of balls (3 x 3 and 3 x 4) for presence and bridging
 - Threshold = 95
 2. Inspect shape of individual balls for consistency
 - Threshold = 95
 - Shape Limit = 1.45
 3. Inspect size of individual balls
 - Threshold = 95
 - Size Range = .400 mm² - .525 mm²
 - Translates to \varnothing range of approx. 0.71 mm – 0.82 mm
 - Loose component ball size is 0.75 mm
 - Average x-ray ball size is .81 mm
 4. Inspect individual balls for voiding (flag if > 10%)
 - Threshold = 75

Shape Limit:

For a perfect circle, the shape value will be 1. As a shape deviates from a perfect circle, the shape value will increase. It is unknown exactly how the value is calculated, but the equipment/software vendor recommends using a shape limit of 2 or less.

Ball Size:

The measured size of the ball in the x-ray image is dependent on several factors:

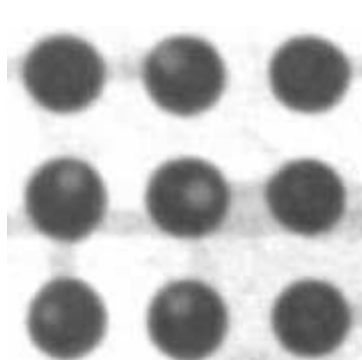
- Original component ball size
- Amount of solder added at assembly
- Weight of component (squish factor)
- X-Ray parameters (power)
- Background (extent to which ball contrasts with surrounding image)
- Threshold value (ball edges are 'feathered', and affected by small changes in threshold)

With some degree of effort, the measured balls size from the x-ray image may be adjusted to match the actual ball size by manipulating the power and threshold settings. This is not necessary, however, and setting relative limits to detect defects on an optimized image is suitable.

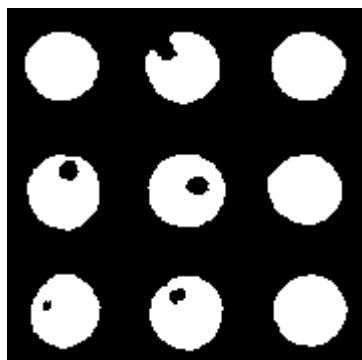
The automated x-ray system applies inspection algorithms to binary images to determine the presence of defects. The inspections include:

- Looking for the expected number of distinct shapes within the inspection area and close to the expected size
- Checking the overall size (diameter / pixel count) of the shapes found
- Checking the 'roundness' of the shapes found
- Looking for and evaluating size of voids within those shapes found

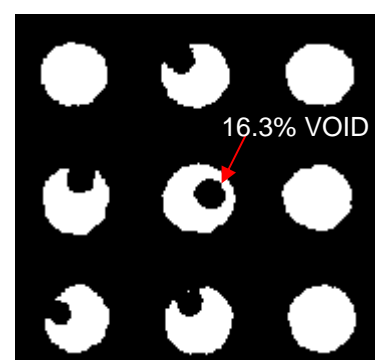
The algorithm requires that a threshold value be set to define what is, and what is not, solder. This will be used to create the binary images from the raw x-ray images. This value is determined by the programmer.



Raw X-Ray Image

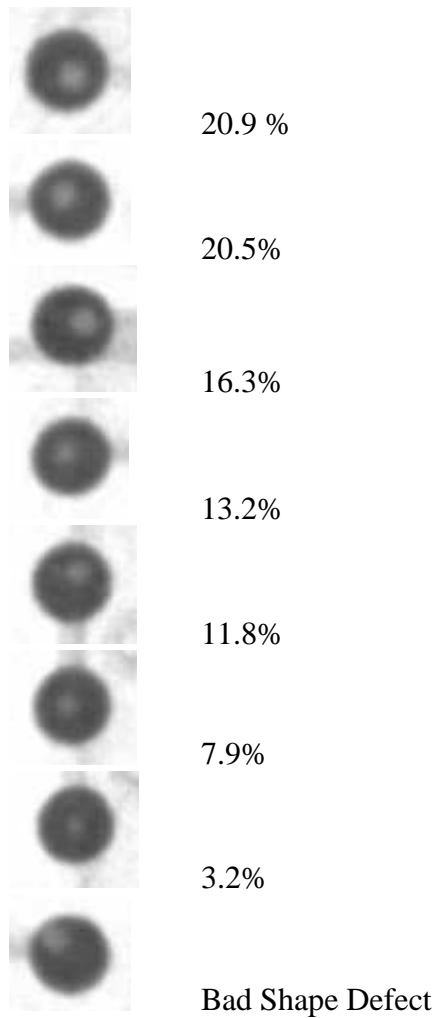


Binary Image for Ball Inspection



Binary Image for Void Inspection

The first image above is the raw x-ray image of part of a BGA. Voids within the solder ball are clearly visible as lighter spots within the joints. The second image is the binary image used to determine the presence, size, and shape of the solder balls. A threshold value has been set (based on the contrast between solder and surrounding areas) for this image such that the resulting shapes in the binary image match the size of the solder balls in the raw x-ray image. The third image is the binary image used to evaluate the presence and size of voids. Because the contrast between the voids and the surrounding solder is different from the contrast between the solder ball and the surrounding area, the threshold level is different, and a different image is created. This threshold value is set such that the resulting voids in the binary image match the size of the voids in the raw x-ray image



Similar to the BGA inspection, the images below are for QFN x-ray inspection. The first image is the raw x-ray image, the second is the binary image for lead bank inspection, and the third is the binary image for void detection. The combined area of the voids shown in this example was calculated at 16%.

